Chap – 5 Introduction to Microprocessors & Organization of 8085

H.S.C. Topic Scope : 21Marks
1 Mark M.C.Q. = 1 = 1x1 = 01
3 Marks Que = 4 = 3x4 = 12
4 Marks Que = 2 = 4x2 = 08

Q1) What is the microprocessor? What are the functions performed by the microprocessor?

Microprocessor definition:

a) Microprocessor is same like CPU of the microcomputer.

b) Microprocessor is register based clock driven electronic device.

c) Microprocessor is a semiconductor, multipurpose, programmable logic device that reads binary instructions from a storage device called as memory and accepts binary data as i/p and processes that data according to the instructions then provides result as o/p.

d) Microprocessor can also viewed as integrated circuit because it have the processing capabilities of large computers, which also performs various computing functions and making decisions to change the sequence of program execution.

Functions performed by the microprocessor:

The following are the different functions performed by the microprocessor during the execution of its process :

a) The microprocessor fetches, decode and execute instruction.

fetching operation: In this operation microprocessor reads op-code of the instruction and stores instruction op-code in instruction register.

decode : In this operation microprocessor decodes an instruction that means it interprets what the op-code i.e. operation performed during execution and what operated data being used for operation etc.

execute: In this operation microprocessor executes the given instruction that means it executes the fetched instruction.

b) Microprocessor transfer data from one block to another block.
e.g. Many such type instructions are provided by microprocessor itself.
Microprocessor transfers data from one block to different I/O lines.
e.g .Many I/O instructions are provided by microprocessor such as
IN, OUT, SIM, RIM etc.

c) Microprocessor gives the proper response to different externally produced interrupts according to their priority. Such as mentioned follows:

d) Microprocessor provides the necessary control and timing signals to the whole system according to the instruction.

Q2) What are the features provided by 8085 microprocessor?

Silent features of Intel 8085 microprocessor:

The main features of microprocessor of 8085 are as listed below:

1) It is a 8-bit microprocessor i.e. 8085 microprocessor can reads or writes or performs arithmetic and logical operations on only 8-bit data at a time. It is designed by NMOS technology.

2) 8085 microprocessor requires a single +5 Volt D.C. power supply.

3) 8085 microprocessor have contains maximum clock frequency upto 3 MHz and minimum clock frequency is upto 500 KHz.

4) 8085 microprocessor has 16 address lines because the width of address bus of microprocessor is 16-bit. So this type processor can accesses 2^{16} =65536=64KB of memory.

5) 8085 microprocessor has 8-bit data bus. So it can generates 8-bit I/O addresses. So that 2^8 = 256 input and 256 output ports can be accessed by 8085 microprocessor..

6) 8085 microprocessor provides five levels of H/W interrupts such as TRAP, RST 7.5, RST 6.5, RST 5.5 and INTR. As well as it provides 8 software interrupts such as RST 0, RST 1, RST 2, RST 3, RST 4, RST 5, RST 6, RST 7.

7) 8085 microprocessor provides two types of serial lines called as serial I/O lines. So that serial peripheral can be interfaced directly with microprocessor of 8085.

8) 8085 microprocessor is a single chip NMOS device implemented using 6200 transistors.

9) 8085 microprocessor provides on-chip clock generator. So that it does not requires external clock generator. But it requires external turned circuit like RC, LC or crystal.

10) 8085 microprocessor requires 2 phases 50% duty cycle of TTL clock.

11) 8085 microprocessor provides on-chip bus controller.

12) 8085 provides different data transfer, arithmetic, logical, branching and machine control as well as stack control instruction which categorized into different addressing modes.

13) 8085 microprocessor is available in 40 pin plastic ceramic DIP package.

14) To selects external memory or I/O devices microprocessor of 8085 uses I/O mapped and I/O system.

15) To communicates with external devices microprocessor uses interrupt method i.e. H/W interrupts.

Q3) Writes a short note on evolution of microprocessor giving one example of each generation?

The microprocessor are evaluated or generated in the five groups as shown below

Evolution of Microprocessor: --→

1) **First Generation :-**

a) In year 1971, the first microprocessor is evaluated in the market called as **Intel's 4004.** Which is 4-bit microprocessor.

b) In year 1972 Intel introduced first general purpose 8-bit microprocessor called as **Intel's 8008.**

b) In year 1973 Motorola introduced **Motorola's 6800.** Which also 8-bit microprocessors.

c) All first generation microprocessor's are designed as PMOS i.e. P-Channel metal oxide semiconductor. Which are generally used in calculator system.

Examples : Intel's 4004 (4-bit), Intel's 8008 (8-bit) ,Motorola's 6800 (8-bit)

2) **Second Generation :-**

a) In year 1974, Intel introduced the first second generation microprocessor called as **Intel's 8080.** Which is 8-bit microprocessor.

b) During second generation the development of microprocessor has been in a direction towards a complete microprocessor system i.e. CPU, RAM, ROM, clock, I/O ports all these are packaged into a single chip. So that in year 1973 , Intel introduced a 8-bit second generation microprocessor called as **Intel's 8085**.

c) In year 1977, 12-bit second generation microprocessor is introduced called as **Intersil's IM 6100** and **Toshiba's T8190**.

Examples : Intel's 8085(8-bit), Intel's 8080(8-bit), Intersil's IM 6100 (12-bit) and Toshiba's T8190 (12-bit) and Zilog's Z80 (8-bit)

3) **Third Generation:-**

a) During third generation direction of microprocessor evolution has been towards one which performs all functions of a minicomputer which can works with bytes, strings of characters etc. So that in year 1978, Intel introduced a first 16-bit advanced microprocessor called as **Intel's 8086**.

b) In year 1979 **Zilog's Z-8000** is introduced which is 16-bit microprocessor.

c) In year 1980 **Motorola's 68000** is introduced which is also 16-bit.
Examples : Intel's 8086, Zilog's Z8000 and Motorola's 68000. All are 16-bit.

4) **Fourth Generation :-**

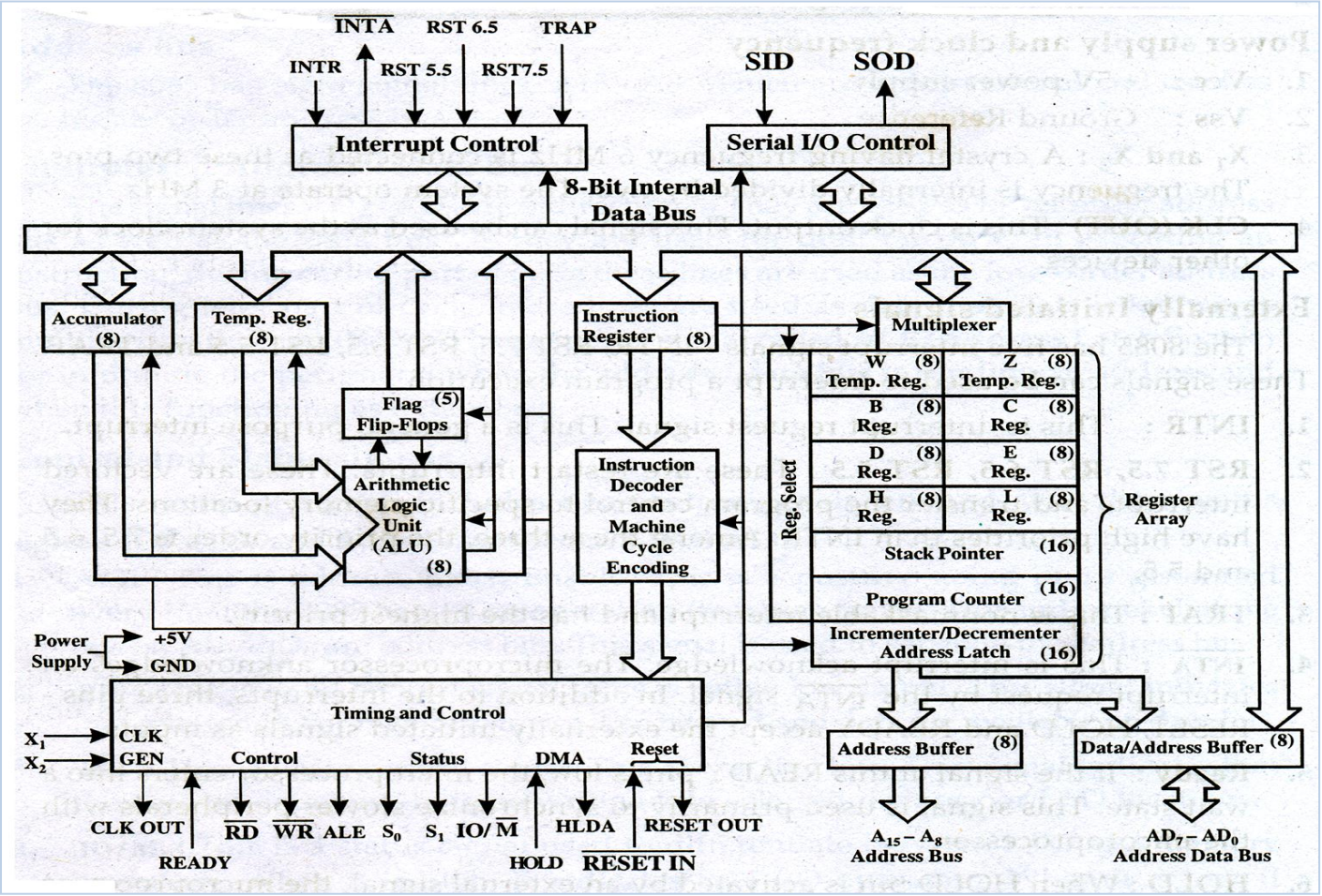
a) In year 1981, Intel introduced first 32-bit fourth generation microprocessor called as **Intel's 80386.** This microprocessor can addressed physical memory of 4 GB.

b) In year 1982 Hewlett Packard i.e. H.P. announces 32-bit microprocessor called as **HP-32**.

c) In year 1987, Motorola introduced 32-bit microprocessor called as **Motorola's 68020.**
Examples : Intel's 80286(16-bit), Intel's 80386(16-bit), Intel's 80486 (32-bit), Motorola's68020 and HP's HP-32.

5) **Fifth Generation :**-During this generation direction towards improvement in speed. Also a system can runs over on new O/S like UNIX, LINUX, WINDOWS etc. So that this generation introduces Pentium microprocessor also known as **Intel's 80586** called as **Pentium-I, Pentium-II,Pentium-III and Pentium-IV** etc. These all processors are 64-bit with physical memory 4GB.
Examples : P-I(64-bit), PII(64-bit), PIII(64-bit), PIV(64-bit)

Q4) Draw a well labeled block functional block diagram of microprocessor 8085? Explain it?



The functional block diagram of 8085 microprocessor includes following types of functional units of block which performs its own functions during executions:

1. ALU organization (ALU unit) 2) Several registers or register array 3) Instruction register
4) Instruction Decoder 5) Timing and control signals 6) Interrupting control signals
7) Serial I/O Controls 8) 8-bit Internal Bus 9) Address Buffer 10) Data/Address Buffer

1. ALU organization : ----→(ALU unit)

The arithmetic and logic unit performs arithmetic, logical and rotating operations. After performing operation the desired result is placed into accumulator. Accumulator, temporary register and flag register is closely associated with ALU. The temporary register is used to hold data during and arithmetic/logic operation. While flag register is used to status operations of ALU, which are set/reset according to result of operation of ALU.

2. Several register/Register of 8085 microprocessor: --→

a. Temporary register :

i) The register W (8-bit) and register Z (8-bit) are known as temporary register.

ii) The temporary register W and Z are only used during arithmetical and logical operations and not for any other purpose.

iii) The temporary registers such as W and Z are used to hold data during an ALU operation i.e. one operand it can hold in ALU operation.

iv) This register is internally used by microprocessor during ALU operation. So that this register can not available for user.

b. General purpose register :------→

i) All general purpose registers are 8-bit registers.

ii) All general purpose registers are available for user that means generally it is used by user in program for transferring data from one to another. So that some times it is also known as programmable registers.

iii) The 8085 microprocessor contains 6 different types of general purpose register such as register B, register C, register D, register E, register H, register L.

iv) When 16-bit data is stored in the form of register then it can be holds into register pair i.e. combination of two registers. The valid register pair of 8085 microprocessor is such as BC register pair, DE register pair, HL register pair.

v) If register pair is BC then its most significant bit i.e. M.S.B. is B register which hold M.S.B. 8-bit data while its least significant i.e. L.S.B. is C register which hold L.S.B. 8-bit data. Similarly If register pair is DE then its most significant bit i.e. M.S.B. is D register which hold M.S.B. 8-bit data while its least significant i.e. L.S.B. is E register which hold L.S.B. 8-bit data. Similarly If register pair is HL then its most significant bit i.e. M.S.B. is H register which hold M.S.B. 8-bit data while its least significant i.e. L.S.B. is L register which hold L.S.B. 8-bit data.

c. Stack pointer: --→.

i. The stack pointer is special 16-bit pointer register which is so called because this register are used to points the memory of stack which reside topper area of RAM.

ii. The SP contains the address of stack top i.e the memory address of last byte entered in stack.

iii. With help of incrementer/decrementer the stack pointer is decremented each time when data is pushed onto stack and incremented each time when data is popped onto the stack.

d) Program Counter : --→

I. The program counter is special 16-bit pointer register which is so called because this register are used to points the memory of next executable instructions.

II. The PC contains the 16 bit address of the memory location where next executable instruction is stored.

III. The microprocessor uses this register to sequence the execution of instruction that means PC deals with sequence of instructions.

IV. The PC is automatically incremented after a particular instruction has been fetched by the MPU i.e. microprocessor unit.

e) Incrementer / Decrementer : --→

i) Incrementer / Decrementer is a 16-bit special purpose register.

ii) This register is used to add or subtract one from the content of program counter or stack pointer.

3. Instruction Register :--→

i) It is a 8-bit register which is not available for user automatically microprocessor internally uses this type of register.

ii) In instruction fetching process that means when instruction takes for execution then the first byte of an instruction is OPCODE is transferred to instruction register that means OPCODE is hold by instruction register during instruction execution period or time.

iii) The content of instruction register then transferred to instruction decoder..

4. Instruction Decoder :--→

i. This is also a 8-bit register which is associative part of instruction register.

ii. During instruction fetching that execution of an instruction the OPCODE is hold into instruction register then for further processing content of instruction register is transferred into instruction decoder.

iii. An instruction decoder decode i.e. interprets the content of instruction register and determines exact steps to be followed in executing the entire instruction.

iv. Thus the O/P of decoder is generated by necessary timing and control signals.

5. Timing and Control signals : --→

i. This section receives the signals from the instruction decoder to determine the nature of an instruction to be executed.

ii. The timing and control lines sends all timing and control signals generated in this to all necessary parts of microprocessor.

6. Interrupting control signals: ---→

i. To communicates peripheral devices or memory devices this signals are used.

ii. These are initiated or initialized external device through h/w or microprocessor itself.

iii An interrupt is an input signal which transfers control to specific routine known as Interrupt Service Routine (ISR) .

7. Serial I/O controls : --→

I Most often I/O devices works with serial data in data transmission.

ii The 8085 has two pins to implement serial transmission SID i.e. Serial Input Data and SOD i.e. Serial Output Data.

iii The 8085 microprocessor's RIM instruction transfers data from SID to bit 7 of an accumulator.

iv A single serial bit may be output via SOD pin of 8085 microprocessor for this it uses SIM instruction.

8. 8-bit internal Bus :--→

This is a pathway for data sending or receiving.

9. Address Buffer : --→

i This is 8-bit unidirectional buffer.

ii This is used to drive higher order address lines i.e. A_8-A_{15}.

10. Data / Address Buffer OR Multiplexed Address/Data Bus Buffer: ---→

i This is an 8-bit bi-directional buffer.

ii This is used to drive multiplexed address/data bus i.e. low-order address bus (A_7-A_0) and data bus ($D_7 – D_0$).

iii It is also used to tri-state the multiplexed address/data bus under certain conditions such as reset, hold, halt and when the bus is not in used.

iv The address/data buffers are used to external addresses and data buses respectively. Due to these buffers the address and data buses can be tri-stated when they are not in use

Q5) Write a short note on flag register of 8085 microprocessor? Explain significance of flag bit with one example?

OR What are flags? Enlist the different flags provided by 8085 microprocessor. Explain when they are set or reset?

OR Define bit pattern of flag register and explain the significance of each flag bit?

a) A flag is defined as a single bit status register .

b) A flag register of 8085 microprocessor is 8-bit register which contains 5 active flags and remaining three flags are undefined/unused/don't care flags.

c) The individual flags of flag register are called as flip-flop that means these are either set or reset by ALU according to the result produced in ALU.

d) The five active flags are such as Sign flag, Zero flag, Auxiliary carry flag, Parity flag and Carry flags.

Bit Number———>	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Flag Name ———>	**S**	**Z**	**X**	**AC**	**X**	**P**	**X**	**CY**

Notification

1) S: Sign Flag
2) Z: Zero Flag
3) AC: Auxiliary Flag
4) P : Parity Flag
5) CY : Carry Flag
6) X : undefined/don't care flag

1) Sign Flag (S) : -

After execution of arithmetic and logic operation, if the most significant bit of the result is 1 then the sign flag is set to 1 otherwise it is 0. If S=1 then this flag determines the result operation is negative i.e number is negative. If S=0 then this flag determines the result of operation is positive i.e. number is positive.

2) Zero Flag (Z) :-

After execution of arithmetic and logic operation, if the result is 0 i.e. Accumulator (A register) contains result 0 then the zero flag is set to 1 otherwise it is 0. If Z=1 then this flag determines the result operation is Zero i.e number is zero. If Z=0 then this flag determines the result of operation is non zero i.e. number non zero..

3) Auxiliary Carry (AC) : -

In arithmetic/logic operation, when carry is generated from bit 3 to bit 4 then auxiliary carry flag is set to 1 otherwise it is zero. If AC=1 then this flag determines the carry is generated from bit 3 to bit 4 in BCD operation. If AC=0 then this flag determines the carry is not generated from bit 3 to bit 4 in BCD operation.

4) Parity Flag (P) :-

After execution of arithmetic/logic operation if Accumulator i.e. A register contains number of 1's is in Even then Parity Flag is set to 1 and if it contains number of 1's is in odd then parity flag reset i.e. 0. If P=1 then this flag determines the result operation is Even i.e number is even. If P=0 then this flag determines the result of operation is odd i.e. number odd..

5) Carry Flag (CY) ;-

If carry(borrow in subtraction) is produced at 9^{th} bit in arithmetic/logic Operation then Carry flag set to 1 otherwise it is reset. If CY=1 then this flag determines the result operation is 9 bit i.e if CY=0 then this flag determines the result of operation is 8-bit.

Uses of Flag in ALU operation:

1) Sign Flag (S) : It is used for determining sign of number i.e. positive or negative. If S=1 then –ve if S=0 then +ve.

2) Zero Flag (Z) : - It is used for determining result is zero or non zero If Z=1 then ACC (A register) = 0 if Z =0 then ACC (A register) = non zero number.

3) **Auxiliary Carry flag (AC) :-** It is used for determining carry is generated from bit 3 to bit 4 in BCD operation i.e. BCD arithmetic only. If AC =1 then carry is generated from bit 3 to bit 4 if AC=0 then carry is not generated from bit 3 to bit 4.

4) **Parity Flag (P) : -** It is used for determining number is even or odd. If in result number of 1's is even then P=1 and if in result number of 1's is odd then P=0

5) **Carry Flag (CY):** It is used for determining carry is generated at bit number 9^{th} or not. In arithmetic operation carry is produced that is 8-bit number produced as 9^{th} bit number then carry flag is set i.e. result is generated as 9^{th} bit otherwise it reset.

Q6) Defines the following terms with suitable diagram:

a) Instruction Cycle b) Machine Cycle c) T-State

a) Instruction Cycle : -

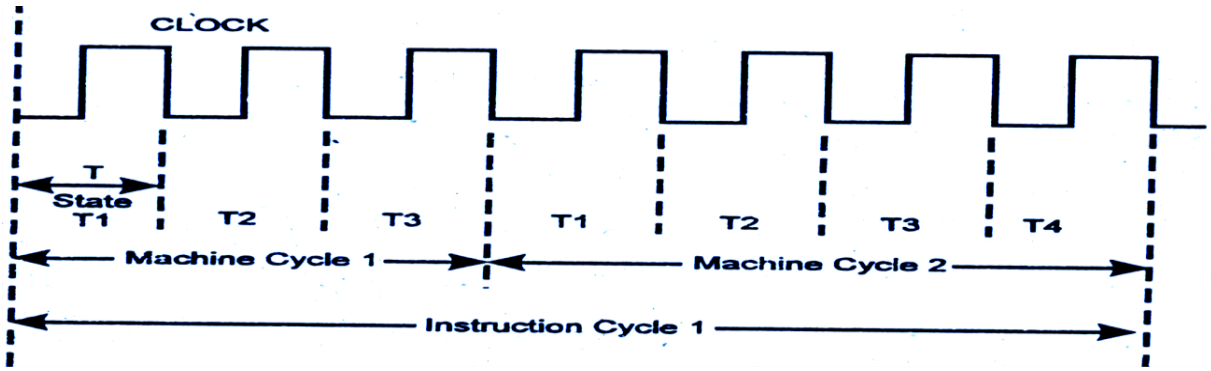
Instruction Cycle is a collection of machine cycles i.e. number of machine cycles forms an instruction cycle. So that an instruction cycle is defined as the time required to complete the execution of an instruction". The 8085 microprocessor instruction cycle consists of min 1 and max.5 machine cycles into one instruction cycle.

b) Machine Cycle :-

Machine Cycle is a collection of T-State i.e. clock periods. So that machine cycle is defined as the time required to complete any operation of accessing either memory or I/O which is the subpart of an instruction". The 8085 microprocessor machine cycle consists of min. 3 and max. 6 T-states into one machine cycle.

c) T-State:-

T-State is subdivision of an operation, which is performed in one clock period is called as T-State.



Importance of T-State and Instruction Cycle :

T-states and instruction cycles are required for execution of an instruction.

Q7) What are I/O mapped I/O and memory mapped I/O schemes? Which one 8085 uses?

OR Write a note on addressing of I/O devices?

Microprocessor is connected to various other devices such as memory and I/O devices. There are two schemes by which these devices can be addressed.

i) **Memory mapped I/O scheme :-**

a) In this addressing scheme same address may not be used for I/O devices as well as for memory location.

b) This scheme has highest priority for I/O device addressing. When this is selected then there is no corresponding information for memory location on address bus.

c) e.g. If suppose address 2000H is for O/P device and whenever this address appears on address bus and is used to selects O/P device then there is no information on memory location 2000H. That means an address 2000H is used to select I/O device as O/P device. So this address is not used for any memory location.

ii) I/O mapped I/O scheme:-

a) In this scheme the same address is used for I/O devices as well as for memory location.

b) 8085 Microprocessor uses I/O mapped I/O scheme to address I/O devices.

c) I/O mapped I/O scheme used in 8085 microprocessor by using status signal pin such as IO / $\overline{M}$. This pin of 8085 microprocessor separates I/O devices operation and memory operation such that. When IO / goes to high state i.e. 1 then it selects addressing for I/O devices and when it goes to low state i.e. 0 then it selects addressing for memory devices.

d) The instruction IN and OUT is used in 8085 microprocessor for I/O addressing.

Q8) What are the different function is carried out on different status of S_0 and S_1 and IO / $\overline{M}$ **?**

The various operations to be carried out are identified by using status signals S_0 and S_1 and IO / $\overline{M}$ as follows

Status Signals			**Machine Cycles status OR Microprocessor operation**
IO / $\overline{M}$	**S_1**	**S_0**	
0	**0**	**1**	**Memory Write**
0	**1**	**0**	**Memory Read**
1	**0**	**1**	**I/O Write**
1	**1**	**0**	**I/O Read**
0	**1**	**1**	**Opcode Fetching**
1	**1**	**1**	**Interrupt acknowledgement**
----	**0**	**0**	**Halt**

Q9) What is an interrupt? What are its types? Explain in detail?

OR What as interrupting system of 8085 microprocessor?

a) An interrupt is a subroutine or subprogram.

b) An interrupts are initiated or executed by either H/W or S/W.

c) When an interrupt are initiated or executed by S/W or microprocessor itself then that interrupts are called as S/W interrupt.

d) When an interrupt are initiated or executed by H/W then that interrupts are called as H/W interrupts.

Importance of Interrupt: - Why interrupts are required/necessary to M.P.U.?

Microprocessor is connected to different peripherals or H/W(s) such as keyboard or LED. So to communicates with these devices M.P.U. (microprocessor unit) i.e. 8085 uses an interrupting method.

What is I.S.R. (interrupt Service Routine) ? OR How interrupts are performs their services?

a) An interrupt performs their services under their own work-space area is called as I.S.R. i.e interrupt service routine.

b) In interrupting an interrupts are as i/p signal which transfers control to specific routine that routine is known as I.S.R.

c) After executing I.S.R. the control is again transfer to main program.

Different types of interrupt? OR Different Interrupting Methods?

According initialization or executing of interrupts, the interrupts are classified into two groups such as below

1. **S/W interrupts**
2. **H/W interrupts**

1. S/W interrupts :

Those interrupts which are initiated or executed through microprocessor itself or by s/w, that interrupts are called as s/w interrupts. Therefore s/w interrupts are not requested by external device or peripheral device or h/w. All S/W interrupts are non-maskable highest priority interrupts.

S/W interrupts are requested by s/w or microprocessor itself means that it is requested by executing interrupt instructions. They can also be requested due to arithmetic errors.

After execution of S/W interrupts program counter is incremented. The microprocessor executes only instruction cycle for executes s/w interrupts that means it does not executes any interrupt acknowledged cycle.

Different Types of S/W interrupts:

The 8085 microprocessor executes s/w interrupts by executing following instructions which are called as its different s/w interrupts.

a) RST 0 b) RST 1 c) RST 2 d) RST 3 e) RST 4 f) RST 5 g) RST 6 h) RST 7

All S/W interrupts are vectored interrupts:

All S/W interrupts are called as vectored interrupts because when these interrupts are given or gets executed or initiated then it is directed or vectored to specific memory location or vector location or fixed location or branching location. That means when these initiates then program control is transferred to main program to fixed location or vector location or branching location i.e. program control jumps to vector address or branching address.

When S/W interrupt called by following instructions then program control transfer such as below :

S/W interrupt or S/W interrupt Instructions	Call location or vector location or branching location or fixed location
RST 0	0 x 8 = 0000 H (in hexadecimal)
RST 1	1 X 8 = 0008 H (in hexadecimal)
RST 2	2 X 8 = 0010 H (in hexadecimal)
RST 3	3 X 8 = 0018 H (in hexadecimal)
RST 4	4 X 8 = 0020 H (in hexadecimal)
RST 5	5 X 8 = 0028 H (in hexadecimal)
RST 6	6 X 8 = 0030 H (in hexadecimal)
RST 7	7 X 8 = 0038 H (in hexadecimal)

2. H/W interrupts :

Those interrupts which are initiated or executed through h/w(s) or peripherals or external devices, that interrupts are called as h/w interrupts.

After execution of H/W interrupts program counter is not incremented. The microprocessor executes interrupt acknowledged cycle to identify which type of hw interrupt is initiated.

H/W interrupts are maskable and non-maskable interrupts?

The maskable interrupts are so called because these interrupts can be masked or made pending using instruction SIM and RIM. The following are maskable h/w interrupts

a. TRAP
b. RST 7.5
c. RST 6.5
d. RST 5.5

The non maskable interrupts are so called because these interrupts can not be masked or made pending. That means it not requested by SIM or RIM instruction. INTR is only one h/w interrupt who is known as non-maskable h/w interrupt.

Different Types of H/W interrupts:

The 8085 microprocessor executes h/w interrupts by requesting peripherals or external devices or h/w(s). The 8085 microprocessor provides the following types of h/w interrupts:

a. TRAP
b. RST 7.5
c. RST 6.5
d. RST 5.5
e. INTR

Vectored H/W interrupts:

H/W interrupts are called as vectored interrupts because when these interrupts are given or gets executed or initiated then it is directed or vectored to specific memory location or vector location or fixed location or branching location. That means when these initiates then program control is transferred to main program to fixed location or vector location or branching location i.e. program control jumps to vector address or branching address.

When H/W interrupt called by following peripherals or external devices then program control is transferred to specific location or fixed location or vectored location or branching location

H/W interrupts	Call location or vector location or branching location or fixed location
TRAP	4.5 x 8 = 0024 H (in hexadecimal)
RST 7.5	7.5 X 8 = 003C H (in hexadecimal)
RST 6.5	6.5 X 8 = 0034 H (in hexadecimal)
RST 5.5	5.5 X 8 = 002C H (in hexadecimal)

Non-Vectored H/W interrupts:

H/W interrupts are called as non vectored interrupts because when these interrupts are given or gets executed or initiated then it does not be directed or vectored to specific memory location or vector location or fixed location or branching location. That means when these initiates then program control is transferred where the main program is addressed i.e. address of program counter .

INTR is a lowest priority non-vectored h/w interrupt when this is initiates then program is executed from program counter address in main program only this interrupt requests to h/w or s/w interrupt and identify which one is initiated then request is transfers to interrupt acknowledge.

Q10) Differentiate between H/W interrupt and S/W interrupts?

H/W interrupt	S/W interrupt
1) Those interrupts which are initiated or executed through h/w(s) or peripherals or external devices, that interrupts are called as h/w interrupts.	1) Those interrupts which are initiated or executed through microprocessor itself or by s/w, with executing restarting instructions from RST 0 to RST 7,that interrupts are called as s/w interrupts.
2) H/W interrupts are used to handles asynchronous events.	2) S/W interrupts are used to handles synchronous events.
3) These interrupts are requested by external or peripheral devices such keyboard and LED.	3) These interrupts are requested by microprocessor itself or s/w interrupt that means these are initiated by executing restart instructions such as RST 0, RST 1, RST 2, RST 3, RST 4 , RST 5, RST 6, RST 7
4) After execution of these interrupts program counter is not incremented.	4) After execution of these interrupts program counter is incremented.
5) The microprocessor executes either interrupt acknowledge cycle or ideal machine cycle to acknowledge h/w interrupts.	5) The microprocessor executes normal instruction cycle to determination or execution or initiating interrupts.
6) These interrupts may be maskable or non-maskable. TRAP, INTR are non maskable and RST 7.5, RST 6.5 and RST 5.5 are maskable interrupts.	6) All S/W interrupts are non-maskable interrupts that means it do not masked by instruction SIM or RIM.
7) H/W interrupts are lower priority interrupts than S/W interrupts.	7) S/W interrupts are highest priority interrupt than H/W interrupt.
8) These interrupts affects on interrupts control logic.	8) S/W interrupt do not affects interrupt control logic.
9) These interrupts improves throughput of the system.	9) These interrupts do not improves throughput of the system.
10) TRAP, RST 7.5, RST 6.5 and INTR are h/w interrupts	10) RST 0, RST 1, RST 2, RST 3, RST 4, RST 5, RST 6, RST 7 are S/W interrupts.

Q11) List H/W interrupts according to their priority and branching/vector address?

The following table shows the priority of H/W interrupts according to highest to lowest as well as it shows its respective vector address or branching address when it goes to execute or initiates:

H/W interrupts	Vector address/Branching address	Priority of H/W interrupt
TRAP	4.5 x 8 = 0024 H (in hexadecimal)	**Highest priority- 1st priority**
RST 7.5	7.5 X 8 = 003C H (in hexadecimal)	**Second Priority**
RST 6.5	6.5 X 8 = 0034 H (in hexadecimal)	**Third Priority**
RST 5.5	5.5 X 8 = 002C H (in hexadecimal)	**Fourth Priority**
INTR	Non vectored	**Lowest priority- 5th priority**

Q12) Differentiate between non-maskable and maskable interrupt?

Non Maskable interrupts	Maskable interrupts
1) Those interrupts which are cannot be masked or cannot made pending when executing instruction SIM or RIM instruction that all interrupts are called as non-maskable interrupts.	1) Those interrupts which is masked or made pending when executing instruction SIM or RIM instruction that all interrupts are called as maskable interrupts.
2) Non maskable interrupts disables all maskable interrupts when initiating.	2) Maskable interrupts cannot disables any non maskable interrupts.
3) Highest priority than maskable interrupts.	3) Lowest priority than non-maskable interrupts.
4) All non maskable interrupts are always vectored interrupts.	4) It may be vectored or non-vectored interrupts
5) Response time for non maskable interrupt is low as compare to maskable	5) Response time for maskable interrupts is high as compares to non maskable.
6) non maskable interrupts are used for emergency purposes like power failure, smoke detector, parity check error etc.	6) maskable interrupts are used to interfacing with peripheral devices.
7) e.g H/W interrupts such as TRAP and INTR are non maskable interrupts. Similarly all S/W interrupts are non maskable interrupts.	7) e.g. H/W interrupts such as RST 7.5, RST 6.5, RST 5.5 are maskable interrupts. No any one of s/w interrupts as maskable interrupts i.e. all s/w interrupts are non-maskable.

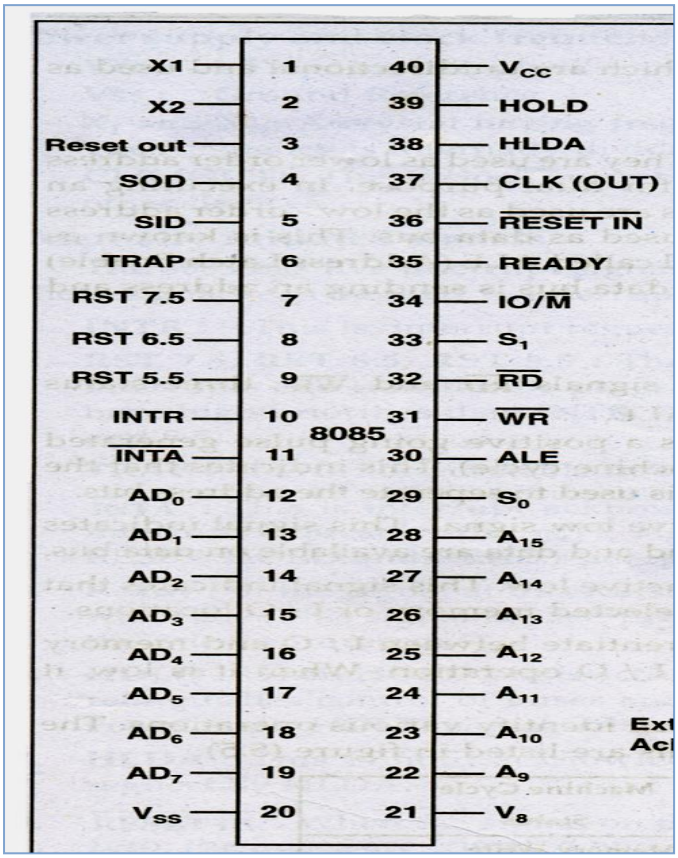
Q13) List S/W interrupts according to their priority and branching/vector address?

The following table shows the priority of S/W interrupts according to highest to lowest as well as it shows its respective vector address or branching address when it goes to execute or initiates:

S/W interrupts	Vector address/Branching address	Priority of H/W interrupt
RST 0	0 x 8 = 0000 H (in hexadecimal)	**Highest priority- 1st priority**
RST 1	1 X 8 = 0008 H (in hexadecimal)	**Second Priority**
RST 2	2 X 8 = 0010 H (in hexadecimal)	**Third Priority**
RST 3	3 X 8 = 0018 H (in hexadecimal)	**Fourth Priority**
RST 4	4 X 8 = 0020 H (in hexadecimal)	**Fifth Priority**
RST 5	5 X 8 = 0028 H (in hexadecimal)	**Sixth Priority**
RST 6	6 X 8 = 0030 H (in hexadecimal)	**Seventh Priority**
RST 7	7 X 8 = 0038 H (in hexadecimal)	**Lowest priority- 8th priority**

Q14) Draw a functional pin diagram of microprocessor 8085?

The 8085 microprocessor is housed in a 40 pin Dual-In-Line-Package i.e. DIP. The pinout diagram for 8085 is shown in following figures



Address Bus & Data Bus pins

1) AD_0-AD_7:

a) These are called as Multiplexed Address/Data Bus pins. That means these are used as lower order address bus i.e. A_0-A_7 and data bus i.e. D_0-D_7.

b) These are 8 bit bidirectional tri-stated pins which carries address as well as data in time shared mode.

c) When these pins are in low state i.e $AD_0 – AD_7$=0 then it carries information of address bus and when these pins are in high state then it carries information of data bus.

d) The term multiplex means first select one and then another.

e) The state of multiplexed address/data bus is depends on ALE state that means ALE informs this pins whether address bus is selected or whether data bus is selected.

2) $A_8 – A_{15}$ Address Bus

a) These are 8-bit output, tri- state signals used to carry higher order address signals of 16-bit address.

b) These are non multiplexed unidirectional address lines.

Status Pins

1) ALE : Address Latch Enable

a) This is an output signal which used to informs that the content on AD_0-AD_7 lines is lower order 8-bit address of 16 bit address when ALE goes high state.

b) When ALE is in LOW state i.e. ALE=0 then it indicates the content on AD_0-AD_7 lines is 8-bit data.

c) ALE signal is used to separates address signals from the data signals i.e. A_0-A_7 and D_0-D_7 from AD_0-AD_7.

2) S_1 and S_0 : Status Signals:

a) These are output status signals used to gives the status of operation performed by the microprocessor. As shown on following conditions.

b) These are not generally used in small system but can be used to generates advance control signals for large system.

S_1	S_0	Operation performed
0	0	HALT
0	1	WRITE
1	0	READ
1	1	FETCH

Control signals :.

1) IO / $\overline{M}$: (Input Output / Memory)

a) This is an output status signal use to give the status of operation performed with memory or I/O by microprocessor.

b) When this pin is in low state i.e. 0 then microprocessor is performing operation with memory and when this pin is in high state i.e. 1 then the microprocessor is performing operation with I/O device.

2) $\overline{RD}$: (Read)

a) This is an active low output control signal used to reads data from memory or I/O device and generated by the microprocessor.

b) If IO / $\overline{M}$ is LOW state i.e. 0 then reads the data from memory and if IO/ is in HIGH state i.e 1 then reads the data from I/O devices.

3) $\overline{WR}$: (Write)

a) This is an active low output control signal used to writes data from memory or I/O device and generated by the microprocessor.

b) If IO / $\overline{M}$ is LOW state i.e. 0 then writes data in memory and if IO/ is in HIGH state i.e 1 then writes data in I/O devices.

Externally Initiated Interrupting pins or signals :

1) READY

a) This is an active high input control signal and used by the microprocessor to checks whether a peripheral is ready or not for data transfer.

b) If READY pin is in HIGH state i.e. 1 then the microprocessor completes the operation and proceeds for next operation.

c) When READY pin is LOW state i.e. 0 then microprocessor will wait until it goes to HIGH state i.e. 1.

d) This is signal is used to synchronize slower peripheral with faster processor.

2) TRAP

a) This is an active high, edge and level triggered, non maskable highest priority H/W interrupt.

b) This signal is used for to interrupting the microprocessor.

c) When TRAP occurs then microprocessor starts their execution from its vector address i.e. fixed location or branching address 0024.(i.e. it is calculated as like TRAP= 4.5X8 = 0024H)

3) RST 7.5, RST 6.5 and RST5.5 (Restart Interrupts) :

a) These are an active high, maskable interrupts.

b) RST 7.5 is edge triggered interrupt while RST 6.5 and RST 5.5 are level triggered interrupts.

c) When RST 7.5, RST 6.5 and RST 5.5 occurs then the microprocessor transfers program control to vector address such as follows

i. When RST 7.5 occurs then it transfers the program control to 003CH i.e it is calculated as like RST 7.5 = 7.5 X 8 = 003CH.

ii. When RST 6.5 occurs then it transfers the program control to 0034H i.e it is calculated as like RST 6.5 = 6.5 X 8 = 0034H.

iii. When RST 5.5 occurs then it transfers the program control to 002CH i.e it is calculated as like RST 5.5 = 5.5 X 8 = 002CH.

4) INTR :

a) INTR is an active high, level triggered general purpose interrupt. INTR means interrupt request.

b) When INTR occurs then the microprocessor generates an interrupt acknowledge signal called as .

c) Among all interrupts INTR has lowest priority. When it goes high then program counter does not increments its content. Immediately the microprocessor suspends its normal sequence of instructions.

5) $\overline{INTA}$:-

a) This is an interrupt acknowledge. The microprocessor acknowledges an interrupt request by the INTA signal.

b) RESET, HOLD and READY pins accepts the externally initiated signals as inputs.

c) At low state INTA indicates that the processor has acknowledged an INTR interrupt.

DMA Request signals:

1) HOLD :

a) HOLD is an active high input signal used to request microprocessor for gaining the control of address, data and control buses.

b) When microprocessor receives HOLD request signal then microprocessor completes operation and release bus control for the other master in the system.

c) While HOLD is DMA request i/p signal it receives signal to HLDA for acknowledging hold request.

2) HLDA

a) It is an active high output hold acknowledgement DMA request signal.

b) It indicates that the HOLD request has been received.

c) After the removal of HOLD request the HLDA goes to low state.

d) When HOLD is acknowledged by HLDA then address bus, data bus, RD, WR, and IO/M are goes to tristate.(i.e. high, low, impedance).

RESETTING signals

1) $\overline{RESETIN}$

a) This is an active low input reset signal.

b) This pin is used to resetting the microprocessor.

c) When this signal is received by the microprocessor then microprocessor clears program counter i.e. program counter address becomes as 0000H location.

d) When this pin is occurred then address, data and control lines become as tri-stated (i.e. high, low, impedance).As well as this signal resets the status of internal registers and flags are unpredictable.

2) RESET OUT

a) This is an active high output signal generated by the microprocessor.

b) After receiving RESET signal then it indicates that the CPU is being reset. Thus this signal is used to reset other devices.

Serial I/O signals :

1) SID (Serial Input data)

a) SID is an active high serial port input signal. It is a data line for serial input.

b) SID pin is used to accepts one bit data under the software control.

c) When RIM instruction is executed then the SID pin data is loaded at D_7 of an accumulator.

2) SOD (Serial Output Data)

b) SOD is an active high serial port output signal. It is a data line for serial output.

c) SOD pin is used to receive one bit data under the software control. That means the 7^{th} bit of an accumulator is outputted on SOD line whenever SIM instruction is takes for execution.

d) When SIM instruction is executed then the SOD pin is set or reset depending on the status of D_7 and D_6 bits of the accumulator.

Power Supply Pins:

1) **V_{cc} :** + 5V D.C. power supply.

2) **V_{ss} :** Ground reference.

Clock Frequency Pins:

1) X_1 and X_2 :

a) These are clock inputs pins which connected to the crystal/LC/RC/LED.

b) The crystal frequency is divided by two and used as operating frequency.

c) The crystal frequency is 6 MHz. So that the operating frequency of 8085 microprocessor is 6 MHz /2 = 3 MHz.

2) CLK(OUT) :

a) This is an output clock signal and used as a system clock.

b) The internal operating frequency is available on this pin is same as the 8085 microprocessor. So that the operating frequency is 3 MHz.

Q15) What are the primary functions of CPU of microcomputer?

The primary functioning unit of any computer system is called as the CPU. Since the primary functions of the CPU of a microcomputer are as follows:

1. Fetch, decode and execute program instructions in the proper order.
2. Transfers data to and from memory and to and from the input/output sections.
3. Responds to external interrupts.
4. Provides overall timing and control signals for the entire system.

Q16) Draw a well labeled block diagram/ functional block diagram of simplified CPU organization? Explain function of each block in detail?

OR **Write a short note on Simplified CPU organization of microcomputer?**

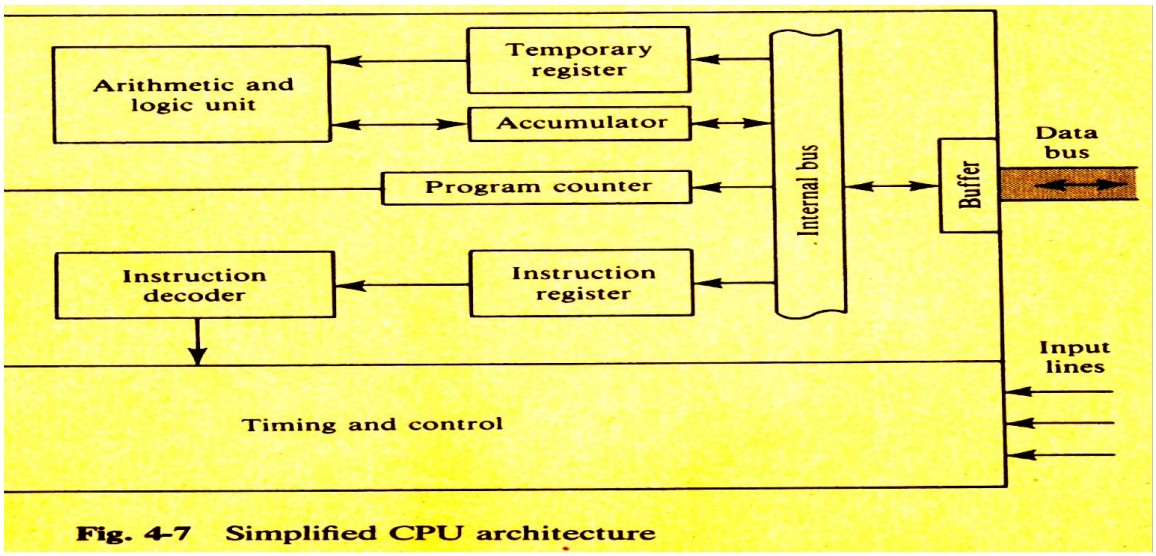


Fig. 4-7 Simplified CPU architecture

The primary functioning unit of any computer system is called as the CPU. Many microprocessor ICs are the CPU of the system. Generally the CPU will contain storage elements called as registers and computational circuitry called the ALU. The CPU will also contains instruction-decoding circuitry and a control and timing section. The CPU will also have the necessary I/O connections.

Functional Blocks/ Units of CPU:-→

The following are functional blocks/ units of CPU :

1) ALU 2) Temporary register 3) Accumulator
4) Program counter 5) Instruction register and instruction decoder
6) Timing and control signals **7)** Buffer/Latch
8) Bus System : a) Address Bus b) Data Bus

1. ALU :

The CPU's arithmetic and logic unit performs operations such as add, shift/rotate, compare, increment, decrement, negate/compliment, ANDing, ORing, XORing, Clear, Preset etc .That means the main process is performed into ALU of CPU's.

2. Temporary register:

This is a one part of ALU which associates to ALU during operation. The temporary registers such as W and Z are used to hold data during an ALU operation i.e. one operand it can hold in ALU operation. This register is internally used by microprocessor during ALU operation. So that this register can not available for user.

3. Accumulator :->

It is a 8-bit primary register. This is a one part of ALU which associates to ALU during operation. It holds one operand during ALU operation. Whenever the ALU performs any arithmetic or logical operation then the processed result i.e. desired result is always stored into accumulator. It can be used both source and destination register. All data transfer between the CPU and I/O devices are performed though an accumulator.

4. Program Counter :-→

a) The program counter is special 16-bit pointer register which is so called because this register are used to points the memory of next executable instructions.

b) The PC contains the 16 bit address of the memory location where next executable instruction is stored.

c) The microprocessor uses this register to sequence the execution of instruction that means PC deals with sequence of instructions.

d) The PC is automatically incremented after a particular instruction has been fetched by the MPU i.e. microprocessor unit.

5. Instruction Register and Instruction Decoder: --→

a) It is a 8-bit register which is not available for user automatically microprocessor internally uses this type of register.

b) In instruction fetching process that means when instruction takes for execution then the first byte of an instruction is OPCODE is transferred to instruction register that means OPCODE is holded by instruction register during instruction execution period or time.

c) The content of instruction register then transferred to instruction decoder.

Instruction Decoder:--→

a) This is also a 8-bit register which is associative part of instruction register.

b) During instruction fetching that execution of an instruction the OPCODE is holded into instruction register then for further processing content of instruction register is transferred into instruction decoder.

c) An instruction decoder decode i.e. interprets the content of instruction register and determines exact steps to be followed in executing the entire instruction.

d) Thus the O/P of decoder is generated by necessary timing and control signals.

6. Timing and Control signals:---→

a) This section receives the signals from the instruction decoder to determine the nature of an instruction to be executed.

b) The timing and control lines sends all timing and control signals generated in this to all necessary parts of microprocessor.

7. Buffer/Latches:--→

a) The buffer and latches are an associative part of internal bus of microprocessor..

b) The buffer are used to enabling latches when they are disabled.

c) The latch is a flip-flop(flag) which is used to stores one bit of information.

8. Bus system :

I) Address Bus : --→

a) The address bus is a group of 16 lines called as addresses which is generally identified as A_0 TO A_{15}.

b) An address bus is a unidirectional bus i.e. data flow in both direction between MPU to peripheral devices.

II) Data Bus : --→

a) The data bus is a group of 8 lines called as data lines or input lines which are generally identified by multiplexed Data/Address lines AD_0-AD_7.

b) Data bus is a bi-directional bus i.e. data flows into both directions between MPU and memory and peripheral.

Primary functions of CPU of microcomputer:---→

The primary functioning unit of any computer system is called as the CPU. Since the primary functions of the CPU of a microcomputer are as follows:

1) Fetch, decode and execute program instructions in the proper order.
2) Transfers data to and from memory and to and from the input/output sections.
3) Responds to external interrupts.
4) Provides overall timing and control signals for the entire system.

Q17) Explain the function of ALU with simple block diagram? Explain the function of each block of ALU? OR Draws a neat labeled diagram of generic ALU and explain its working?

OR Explain the organization of ALU with the help of simple block diagram?

Functions of ALU :-

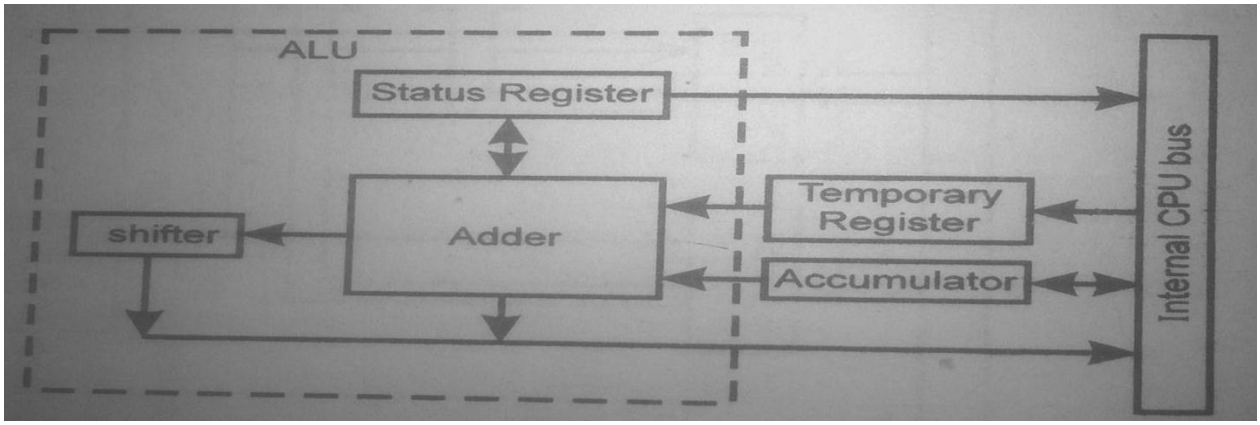
The Arithmetic & Logic Unit performs following such type of different functions

1) The ALU is a 8-bit because 8085 microprocessor is always 8-bit. So that ALU is capable of accepting 8-bit and receiving 8-bit data.
2) ALU performs arithmetic, logic and rotate operations. The desired result is typically stored into accumulator.
3) Accumulator, temporary register and flag register is closely associated with ALU during ALU operation.
4) The temporary register and accumulator is used to hold one operand during an ALU operation.
5) The flag register and always set or reset according to the result of operation in ALU.
6) The binary adder of ALU performs all arithmetic operations like addition, subtraction, increment, decrement etc. with the result being fed back into the accumulator via internal bus.
7) The shifter of ALU performs all logical operations like rotating/shifting, comparing, logical ANDing, logical ORing, logical XORing etc. Result is again placed into the accumulator.

Organization of ALU : -

The above figure shows the functional sections of ALU. The ALU of 8085 microprocessor/ generic microprocessor contains following type of units of ALU:

a) Binary Adder b) Shifter c) Status Register



a) **Binary Adder :**

This is a one unit of ALU. This unit of ALU performs all arithmetic operations like addition, subtraction, increment, decrement etc. and the result of ALU always stored into the accumulator via internal bus.

b) **Shifter :**

This is a one part of ALU. This unit of ALU performs all logical operations like rotating/shifting, comparing, logical ANDing, logical ORing, logical XORing etc. Result is again placed into the accumulator.

c) **Status Register:**

This is one part of ALU. This is also called as flip-flop or flag register or psw (program status word) or condition code register when condition is being specified on using individual flags in branching instructions.

The status register of ALU contains group of five individual flags called as flip-flop such as cy flag, sign flag, zero flag, auxiliary carry flag, parity flag, which are set (1) or reset (0) based on condition created by the last ALU operation i.e. on content of ALU these are set or reset.

Temporary Register : -

This is a one part of ALU which associates to ALU during operation. The temporary registers such as W and Z are used to hold data during an ALU operation i.e. one operand it can hold in ALU operation. This register is internally used by microprocessor during ALU operation. So that this register can not available for user.

Accumulator :

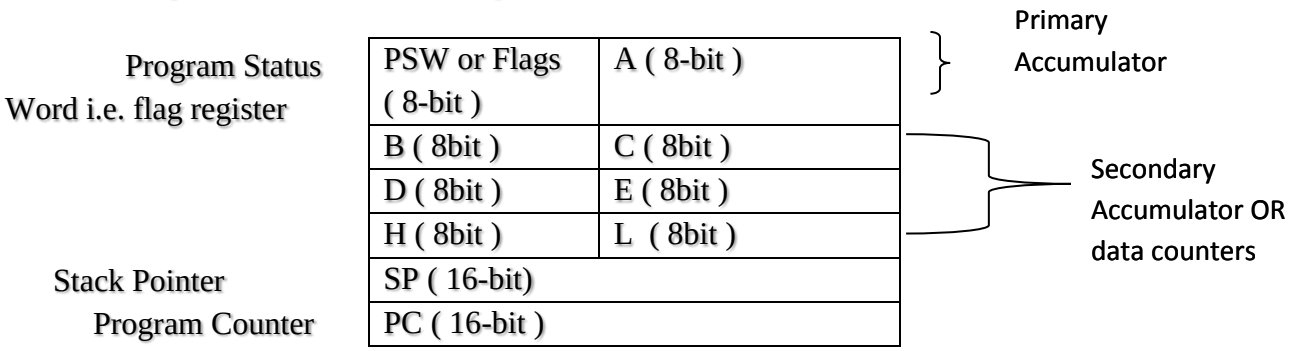
It is a 8-bit primary register. This is a one part of ALU which associates to ALU during operation. It holds one operand during ALU operation. Whenever the ALU performs any arithmetic or logical operation then the processed result i.e. desired result is always stored into accumulator. It can be used both source and destination register. All data transfer between the CPU and I/O devices are performed though an accumulator.

Internal CPU bus:

This system bus of ALU. This contains three types of data bus, address bus and control buses etc. This buses are used in ALU operation as pathway that means whenever binary adder of ALU performs all arithmetic operation then result processed in ALU transfers to accumulator via internal bus. Similarly when shifter of ALU performs all logical operation then result processed in ALU transfers to accumulator via internal bus.

Q18) Draws the diagram of CPU registers of Intel 8085 with function of each register in detail?

The CPU register of Intel 8085 microprocessor is as follows :



The 8085 microprocessor unit (MPU) uses both type of 8-bit and 16-bit registers are used. The 8085 microprocessor has 8 addressable 8-bit registers being these registers 6 registers can be used as 8-bit registers the registers such as B, C, D, E, H and L . These all registers are also used as 16-bit whenever it is paired into register pair. The possible register pairs are such as BC rp/DE rp/HL rp and In addition the remaining two register such as SP and PC are used as 16-bit registers.

PSW/Flag register/Status register:

This is one part of ALU. This is also called as flip-flop or flag register or psw (program status word) or condition code register when condition is being specified on using individual flags in branching instructions.

The status register of ALU contains group of five individual flags called as flip-flop such as cy flag, sign flag, zero flag, auxiliary carry flag, parity flag, which are set (1) or reset (0) based on condition created by the last ALU operation i.e. on content of ALU these are set or reset.

The PSW of microprocessor is program status word which is a combination of two 8-bit registers. The Accumulator of microprocessor is a 8-bit high order register of PSW, while flag register is 8-bit low order register of PSW. This registers are also generally used conditional jump, call, return and stack related instructions.

Accumulator :

It is a 8-bit primary register. This is a one part of ALU which associates to ALU during operation. It holds one operand during ALU operation. Whenever the ALU performs any arithmetic or logical operation then the processed result i.e. desired result is always stored into accumulator. It can be used both source and destination register. All data transfer between the CPU and I/O devices are performed though an accumulator.

B and C register:

a) The register B or C is a general purpose/secondary accumulator/data counter register.
b) These are programmable means programmer can used them to load or transfers data from one to another.
c) These register are generally used to loads or stores data from one register to another register or one memory to register or one register to I/O devices.
d) This register are called general purpose because these are easily available for user.
e) The register B or C is a 8-bit register that means it accept or receives 8-bit data.

f) B and C register are also used as 16-bit register while these are paired into register. The register pair of B and C register is known as BC rp which holds 16-bit data. The most significant 8-bit data i.e. MSB data i.e high order data is stored into B register because B register is a high order 8-bit register of BC rp. Whereas the least significant 8-bit data i.e. LSB data i.e low order data is stored into C register because C register is a low order 8-bit register of BC rp

g) Whenever the B and C register are paired into register pair then it is hold 16 bit data so this is known as BC register paired addressed memory location.

D and E register:

a) The register D or E is a general purpose/secondary accumulator/data counter register.

b) These are programmable means programmer can used them to load or transfers data from one to another.

c) These register are generally used to loads or stores data from one register to another register or one memory to register or one register to I/O devices.

d) This register are called general purpose because these are easily available for user.

e) The register D or E is a 8-bit register that means it accept or receives 8-bit data.

f) D and E register are also used as 16-bit register while these are paired into register. The register pair of D and E register is known as DE rp which holds 16-bit data. The most significant 8-bit data i.e. MSB data i.e high order data is stored into D register because D register is a high order 8-bit register of DE rp. Whereas the least significant 8-bit data i.e. LSB data i.e low order data is stored into E register because E register is a low order 8-bit register of DE rp

g) Whenever the D and E register are paired into register pair then it is hold 16 bit data so this is known as DE register paired addressed memory location.

H and L register:

a) The register H or L is a general purpose/secondary accumulator/data counter register.

b) These are programmable means programmer can used them to load or transfers data from one to another.

c) These register are generally used to loads or stores data from one register to another register or one memory to register or one register to I/O devices.

d) This register are called general purpose because these are easily available for user.

e) The register H or L is a 8-bit register that means it accept or receives 8-bit data.

f) H and L register are also used as 16-bit register while these are paired into register. The register pair of H and L register is known as HL rp which holds 16-bit data. The most significant 8-bit data i.e. MSB data i.e high order data is stored into H register because H register is a high order 8-bit register of HL rp. Whereas the least significant 8-bit data i.e. LSB data i.e low order data is stored into L register because L register is a low order 8-bit register of HL rp

g) Whenever the H and L register are paired into register pair then it is hold 16 bit data so this is known as HL register paired addressed memory location.

Stack Pointer (SP) :-

a) The stack pointer is special 16-bit pointer register which is so called because this register are used to points the memory of stack which reside topper area of RAM.

b) The SP contains the address of stack top i.e the memory address of last byte entered in stack.

c) With help of incrementer/decrementer the stack pointer is decremented each time when data is pushed onto stack and incremented each time when data is popped onto the stack.

Program Counter (PC) :-

a) The program counter is special 16-bit pointer register which is so called because this register are used to points the memory of next executable instructions.

b) The PC contains the 16 bit address of the memory location where next executable instruction is stored.

c) The microprocessor uses this register to sequence the execution of instruction that means PC deals with sequence of instructions.

d) The PC is automatically incremented after a particular instruction has been fetched by the MPU i.e. microprocessor unit.

Q19) Draw a well labeled diagram of microprocessor based system? Describe in brief all blocks?

Microcomputer is one of the microprocessor based systems. The structure of microcomputer is mentioned in above figure. The microprocessor is a semiconductor device consisting of electronic logic circuits. It is capable of performing various computing functions and making decisions to change the sequence of program execution.

The microprocessor can be broadly divided into three parts such as mentioned follows:

1. Arithmetic / Logic Unit
2. Registers
3. Control unit

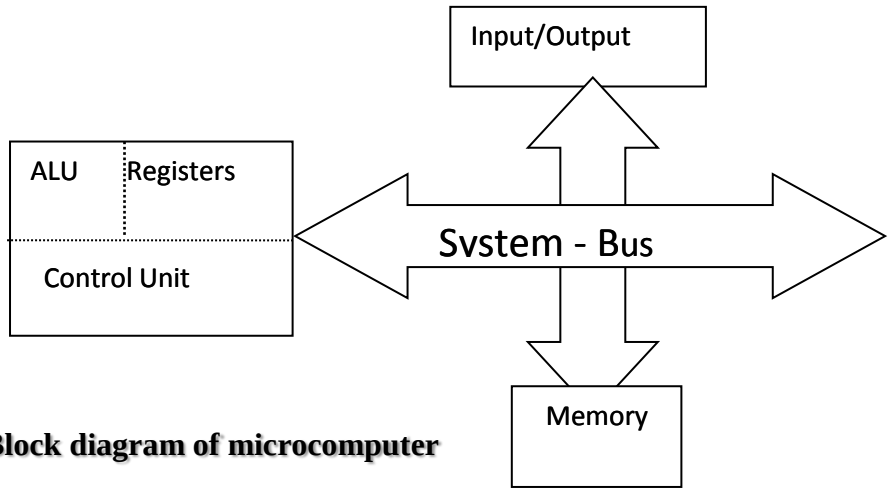


Fig : Microprocessor Based System/ Block diagram of microcomputer

1. Arithmetic / Logic Unit : (ALU)

This is the area of the microprocessor where various computing functions are performed on the data. The ALU unit performs such arithmetic operations as addition and subtraction, logic operations such as AND, OR and Exclusive OR. Then the desired results are stored either into registers or into memory.

2. Registers :

This area of microprocessor consists of various registers. These registers are primarily used to stores data temporarily during the execution of program. Some of the registers are accessible to the user through instructions.

3. Control Unit :

The control unit provides the necessary timing and control signals to all the operations in the microcomputer. It controls the flow of data between the microcomputer and memory and peripherals.

4. Memory :

The memory stores binary information such as instructons and data then it provides that information to the microprocessor whenever necessary. To executes programs the microprocessor reads instructions and data from memory and performs computing operations in its ALU section. The results then either transferred to the output section for display or stored in memory for later use.

5. Input / Output (I/O) :

This section communicates with outside world. I/O devices are known as peripherals. The I/P devices such as keyboard switches to an analog to digital converter. These devices then are used to transfer data from outside world to microprocessor.

The O/P devices such as LED's i.e. Light Emitting Diode or CRT i.e. Cathode Ray Tube or video screen or printer or plotter or magnetic tape or digital to analog converter. These devices then transfers data from microprocessor to the outside world. The data can be displayed on CRT or video screen and it can be printed on paper by using printer.

6. System bus:

The system bus is a communication path between the microprocessor and peripherals. It is a group of wires to carry bits. These are several buses in the system.

Q20) Draw a well labeled block diagram of generic/general microprocessor? Explain its functional units?

Microprocessor is primary functioning unit. The figure shows the detailed block diagram of generic microprocessor i.e. general microprocessor. It consists following block/units:

1. Arithmetic and Logic Unit & its associate blocks 2. Several registers
3. Timing and control section 4. Bus buffer and Latches 5. Interrupt control

1. Arithmetic and Logic Unit and its associative blocks:

The arithmetic and logic unit performs arithmetic, logical and rotating operations.

After performing operation the desired result is placed into accumulator. Accumulator, temporary register and flag register is closely associated with ALU. The temporary register is used to hold data during and arithmetic/logic operation. While flag register is used to status operations of ALU, which are set/reset according to result of operation of ALU.

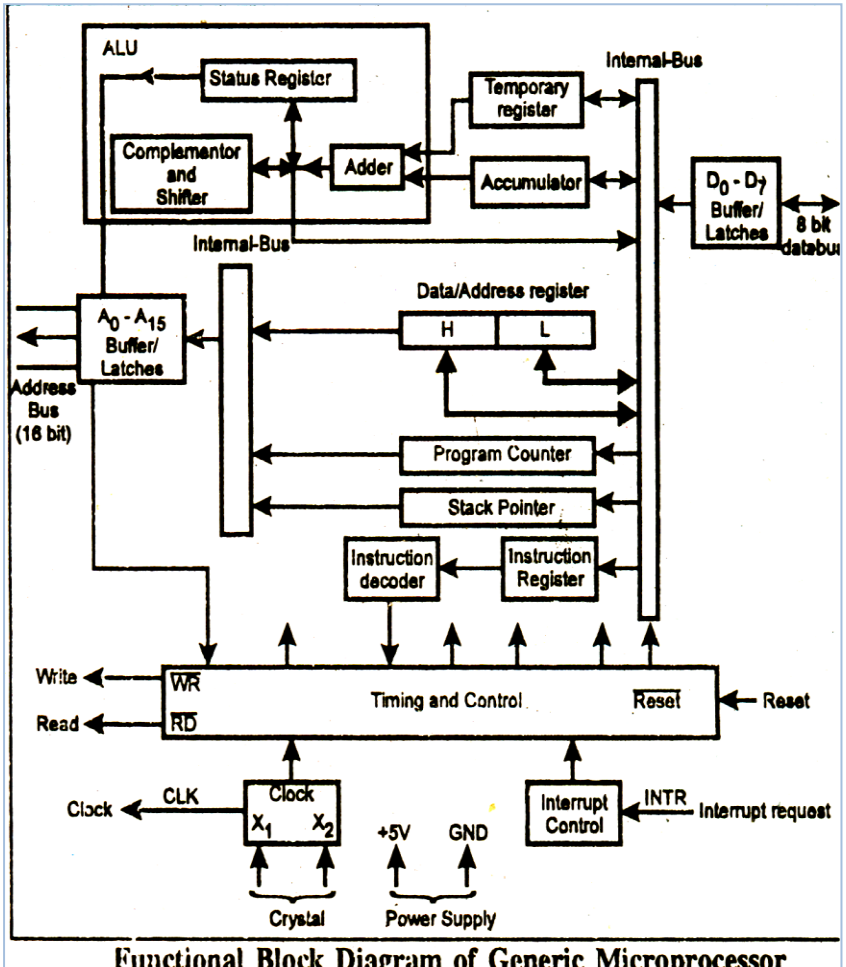
Associative blocks of ALU :

a. <u>Status register</u>

This is one part of ALU. This is also called as flip-flop or flag register or psw (program status word) or condition code register when condition is being specified on using individual flags in branching instructions.

The status register of ALU contains group of five individual flags called as flip-flop such as cy flag, sign flag, zero flag, auxiliary carry flag, parity flag, which are set (1) or reset (0) based on condition created by the last ALU operation i.e. on content of ALU these are set or reset.

The PSW of microprocessor is program status word which is a combination of two 8-bit registers. The Accumulator of microprocessor is a 8-bit high order register of PSW, while flag register is 8-bit low order register of PSW.



Functional Block Diagram of Generic Microprocessor

This registers are also generally used conditional jump, call, return and stack related instructions.

b. Temporary register

This is a one part of ALU which associates to ALU during operation. The temporary registers such as W and Z are used to hold data during an ALU operation i.e. one operand it can hold in ALU operation. This register is internally used by microprocessor during ALU operation. So that this register can not available for user.

c. Accumulator

It is a 8-bit primary register. This is a one part of ALU which associates to ALU during operation. It holds one operand during ALU operation. Whenever the ALU performs any arithmetic or logical operation then the processed result i.e. desired result is always stored into accumulator. It can be used both source and destination register. All data transfer between the CPU and I/O devices are performed though an accumulator.

d. Adder

This is a one unit of ALU. This unit of ALU performs all arithmetic operations like addition, subtraction, increment, decrement etc. and the result of ALU always stored into the accumulator via internal bus.

e. Complementer and Shifter

. This is a one part of ALU. This unit of ALU performs all logical operations like rotating/shifting, comparing, logical ANDing, logical ORing, logical XORing etc. Result is again placed into the accumulator.

2. Several registers of generic microprocessor :

a. Data/Address register:

i) The data/address register name suggest that this can be used separately or as a combined pair.

ii) H/L register is a data/address register.

iii) When H or L is used separately then it is known data register which is capable to hold 8-bit data. While it is used in pair then it is known HL pair and also known as address register.

b. Program Counter

1. The program counter is special 16-bit pointer register which is so called because this register are used to points the memory of next executable instructions.
2. The PC contains the 16 bit address of the memory location where next executable instruction is stored.
3. The microprocessor uses this register to sequence the execution of instruction that means PC deals with sequence of instructions.
4. The PC is automatically incremented after a particular instruction has been fetched by the MPU i.e. microprocessor unit.

c. Stack Pointer

1. The stack pointer is special 16-bit pointer register which is so called because this register are used to points the memory of stack which reside topper area of RAM.
2. The SP contains the address of stack top i.e the memory address of last byte entered in stack.
3. With help of incrementer/decrementer the stack pointer is decremented each time when data is pushed onto stack and incremented each

d. Instruction Register

1. It is a 8-bit register which is not available for user automatically microprocessor internally uses this type of register.
2. In instruction fetching process that means when instruction takes for execution then the first byte of an instruction is OPCODE is transferred to instruction register that means OPCODE is holded by instruction register during instruction execution period or time.
3. The content of instruction register then transferred to instruction decoder.

e. Instruction Decoder

1. This is also a 8-bit register which is associative part of instruction register.
2. During instruction fetching that execution of an instruction the OPCODE is holded into instruction register then for further processing content of instruction register is transferred into instruction decoder.
3. An instruction decoder decode i.e. interprets the content of instruction register and determines exact steps to be followed in executing the entire instruction.
4. Thus the O/P of decoder is generated by necessary timing and control signals.

3. Timing and Control signals:---→

1. This section receives the signals from the instruction decoder to determine the nature of an instruction to be executed.
2. The timing and control lines sends all timing and control signals generated in this to all necessary parts of microprocessor.

4. Buffer/Latches:--→

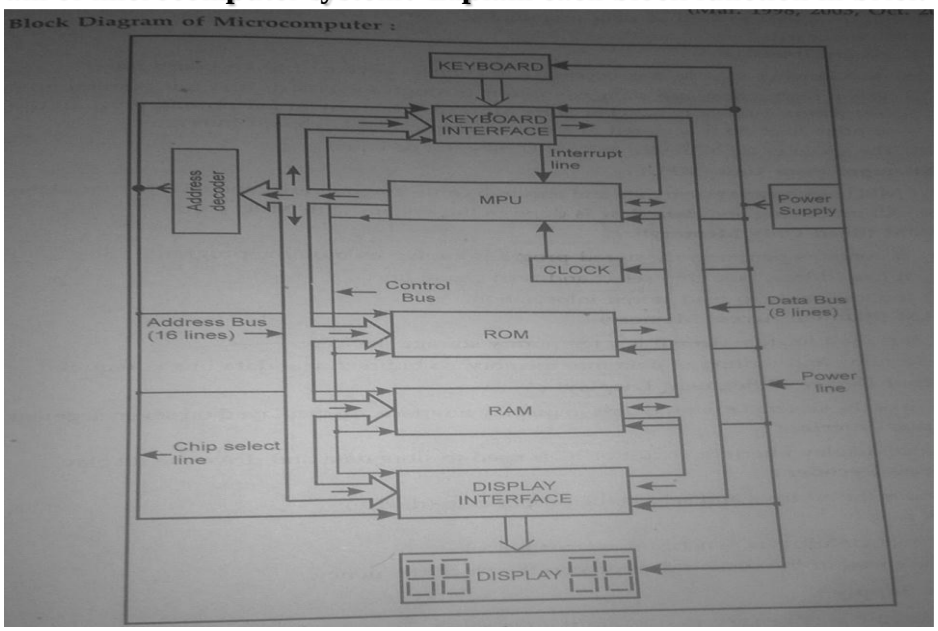
1. The buffer and latches are an associative part of internal bus of microprocessor..
2. The buffer are used to enabling latches when they are disabled.
3. The latch is a flip-flop(flag) which is used to stores one bit of information.

5. Interrupting control signals: ---→

i. To communicates peripheral devices or memory devices this signals are used.
ii. These are initiated or initialized external device through h/w or microprocessor itself.
iii An interrupt is an input signal which transfers control to specific routine known as Interrupt Service Routine (ISR) .

Q21) Draws a well-labeled block diagram of microcomputer system? Explain each block function in detail? OR Draws a structure of microcomputer and describe in detail?

OR Draw a block diagram of microcomputer system? Explain each block function in brief.



Micro computer mainly contains following blocks :

1) Input device (keyboard) 2) Microprocessor unit 3) Program Memory (ROM)
4) Data memory (RAM) 5) Output device (7-segment display)

1) Input device (keyboard) :-

The data is entered or input by keyboard. The keyboard contains keyboard interface.

* Keyboard Interface :-

Due to following reasons it is necessary to connect keyboard to keyboard interface:

a) When instruction and data is entered through keyboard, it is not possible to feed the instruction directly to MPU because MPU may be busy in performing previous instruction or other task. So that it is stored in a special chip called as keyboard interface.

b) The speed of input device and MPU may not be equal.

2) Microprocessor unit (MPU) :-

i) MPU processed system data and required control signals are generated to control the system.

ii) All processing and data flow is done in the system with MPU chip.

3) Program Memory (Read Only Memory) :-

i) It contains permanently stored program known as monitor program.

ii) It has address bus chip which select and read signal line.

iii) It allows only to read stored information.

4) Data memory (Random Access Memory) :-

i) It is used to store data. It is a temporary storage device.

ii) Reading and Writing data into memory, so bidirectional data bus is required.

5) Output device (7-segment display) :-

Output of the system i.e. stored data in display interface are displayed on seven segment display. This contains a display interface. The display interface is circuit or IC is used to store data and drive the display.

6) Address decoder :-

It decodes the address and selects the proper chip or device.

7) Clock :-

i) Whole circuitry is synchronized with clock.

ii) The speed of the system is depends on the clock frequency.

8) Power supply :-

It is necessary to operate the circuit.

9) Interrupt line :-

It is used to interrupt the MPU.

10) Address bus:-

It is 16 bit address bus. It is unidirectional from the MPU is used to flow bits of required memory to devices.

11) Data bus :-

It is 8 bit bidirectional bus. It is used to transfer data among MPU and devices.

12) Control bus :-

It carries control signals generated by MPU.

13) Power line :

It is necessary to operate the circuit.

Q22) What is multiplexed BUS in 8085? Give its advantages.

Microprocessor 8085 has 8 bit data bus and 16 bit address bus. The 8bit LSB of address bus are passed on the same eight lines as that of data bus i.e. on the signal lines AD_7-AD_0. These signal lines are bi directional. They are used for dual purpose for LSB of 8 bit of address and as well as 8 bit data. This is known as multiplexing and such bus is known as multiplexed bus.

To multiplexed means first to select one and then other. In executing an instruction during earlier part of cycle these lines are used as the LSB address bus. During later part of cycle these lines are used as data bus.

The 8085 has a special signal called ALE for informing the peripheral when the address/data bus is sending address and when it is functioning as a data bus. If signal of pin ALE is 1 i.e. high then the bits on AD_7-AD_0 are address bit else they are data bits.

Advantages of multiplexed BUS:

1) These performs dual function at one memory location such as it first use of the bus is send the address and next to send or receive data via same bus.
2) It interacts between data bus and address bus ALE status is used.
3) It select I/O devices and memory devices for reading and writing data.

H.S.C. Board Question Bank
1 Mark Objective Type question Bank

1. The invalid register pair for 8085 microprocessor is ---------- M2002, M2005
   a) BC b) HL c) SP d) DE
   Ans The invalid register pair for 8085 microprocessor is SP.
2. CPU generally contains storage device is called ------ O2002
   a) Registers b) ALU c) timing & control d) Counter
   Ans CPU generally contains storage device is called Registers
3. In the flag register of 8085 microprocessor ---------- number of bits are kept unused O2003
   a) 5 b) 3 c) 4 d) 2
   Ans In the flag register of 8085 microprocessor 3 number of bits are kept unused
4. In 8085 microprocessor serial data from external device is received on ---------- pin M2004
   a) SID b) SOD c) HOLD d) READY
   Ans In 8085 microprocessor serial data from external device is received on SID pin
5. ------- is not a vectored interrupt O2004
   a) TRAP b) INTR c) RST 7.5 d) RST 6.5
   Ans : INTR is not a vectored interrupt
6. ---------- flag bit us reset when flag register content is D4H. M2006
   a) S b) Z c) CY d) AC
   Ans: CY flag bit us reset when flag register content is D4H.
7. -------- register of 8085 microprocessor is only used during arithmetical and logical operations and not for any other purpose. O2006
   a) ACC b) B c) TEMP d) SP
   Ans : TEMP register of 8085 microprocessor is only used during arithmetical and logical operations and not for any other purpose.
8. ------- bus is one way data path from MPU to all devices M2008
   a) Data b) Address c) Control d) None of these
   Ans : Address bus is one way data path from MPU to all devices

3 Mark Type question Bank

M2002

1) Write a short note on evolution of microprocessor giving one example of each generation
2) List any three primary functions of CPU of microcomputer
3) Define following terms with suitable diagram:
   a) Instruction cycle b) Machine cycle c) T-state
4) Describe in brief function of following pins in 8085 microprocessor:
   a) HOLD b) INTR c) $\overline{RESETIN}$

M2003

1) Describe the following registers of 8085 microprocessor:
   a) Program counter b) Stack Pointer c) Accumulator
2) Explain the function of the following pins of 8085:
   a) HOLD b) $\overline{RESETIN}$ c) IO/$\overline{M}$
3) what is a flag register? In its use in ALU operations giving one example.

O2003

1) Draw a neat labeled block diagram of a generic microprocessor
2) Write a short note on evolution of microprocessors. Give one example of each generation
3) List any three primary functions of the CPU of a microcomputer
4) Describe in brief the function of following pins in 8085 microprocessor:
   a) HLDA b) READY c) RST 7.5

M2004

1) Explain the organization of ALU with simple block diagram.
2) Explain the function of the following registers of 8085 microprocessor:
   a) Instruction register b) Accumulator c) Program Counter
3) Explain the sign and parity flags of 8085 microprocessor with suitable example.
4) Describe in brief the function of the following pins of 8085 microprocessor:
   a) RESETOUT b) HLDA c) IO/$\overline{M}$

O2004

1) Write a note on evolution of microprocessor giving one example of each evolution
2) Draw a neat labeled pin diagram of 8085 microprocessor
3) Explain the following terms:
   a) T-state b) Machine cycle c) Instruction Cycle
4) Explain the following :
   a) Instruction register b) Program counter c) Accumulator

M2005

1) Draw a neat labeled diagram of a generic microprocessor
2) Write a short note on evolution of microprocessor giving one example of each generation
3) Describe in brief the function of following pins of 8085 microprocessor:
   a) TRAP b) $\overline{WR}$ c) ALE
4) Define the following terms with suitable diagram:
   a) Instruction cycle b) Machine cycle c) T-states

O2005

1) Draw a diagram of CPU registers of Intel 8085 with function of each register
2) What is interrupt? Why the interrupt signals are used by peripheral device? What is non-maskable interrupt?
3) Explain the function of the following pins of Intel 8085 microprocessor :
   a) ALE b) $\overline{INTA}$ c) READY

4) Explain the use of stack and stack pointer register in Intel 8085 microprocessor
5) List any three primary functions of CPU of microcomputer

M2006

1) Describe in brief the functions of the following pins of 8085:
   a) $\overline{RD}$ b) CLKOUT c) ALE
2) Explain the working of generic ALU with a suitable example.
3) Explain the following blocks of 8085 microprocessor :
   a) Serial I/O control b) Accumulator c) Multiplexed Address/Data Bus Buffer
4) Draw bit pattern of flag register and explain the significance of each flag bit.

O2006

1) Explain the read/write operation with reference to IO/$\overline{M}$, S_0 and S_1 pins of IC 8085.
2) Draw a neat labeled diagram of generic microprocessor.
3) If flag register contents are C1H and 84H then interpret its meaning separately.
4) Explain the following registers f 8085 :
   a) IR b) SP c) PC
5) Explain the following terms with suitable diagram:
   a) Fetch Cycle b) Instruction Cycle c) Machine Cycle

M2007

1) What do you mean by scratch pad register in Intel 8085 microprocessor
2) Define : i) PSW ii) MAR iii) Stack pointer
3) Give the function of following :
   a) Multiplexed bus AD_0-AD_7 b) S_0, S_1 and IO/$\overline{M}$
   c) HOLD and HLDA pins of Intel 8085 microprocessor

O2007

1) Write a short note evolution of microprocessor.
2) Explain the function of the following with respect to 8085 microprocessor:
   a) Instruction Decoder b) ALU c) Three Bus Structure
3) Write a short note on flag in 8085 microprocessor.
4) Describe in brief the function of the following pins of 8085 microprocessor:
   a) ALE b) $\overline{RESETIN}$ c) SOD

M2008

1) Draw a neat labeled functional block diagram of 8085 microprocessor.
2) Write a short note on evolution of microprocessor giving one example of each generation
3) Write the features of 8085 microprocessor.
4) Describe in brief the function of the following pins of 8085 microprocessor :
   a) HLDA b) READY c) RST 7.5
5) List any three primary functions of the CPU of the microcomputer.

4 Mark Type question Bank

M2002

1) Write the function of following units in microprocessor:
   a) ALU b) Stack pointer c) Instruction Register and Decoder
2) The flag register of 8085 microprocessor contains the data 45H. Interpre it's meaning.

M2003

1) Draw block diagram of a microcomputer. Explain function of each block in short.
2) Write a note on evolution of microprocessor.

O2003

1) Write the function of following units on the microprocessor of 8085:

a) Accumulator b) Stack Pointer c) Instruction Decoderd) Serial I/O control

2) Write a short note on flag register of 8085 microprocessor. Explain the significance of flag bits with one example.

M2004

1) Explain in brief the four primary functions of the CPU of a microcomputer.
2) In 8085 microprocessor, the flag register content is 3CH, interpret's its meaning.

O2004

1) What is a vectored interrupt? What is a non-maskable interrupt? State all hardware interrupts with their priorities and branching addresses.

M2005

1) Write the function of following units in 8085 microprocessor:
   a) Accumulator b) Stack pointer c) Instruction Decoderd) Serial I/O controller
2) The flag register of 8085 microprocessor contains data B5H. Interpret's its meaning.

M2006

1) Explain the four primary functions of a generic microprocessor.
2) List all hardware interrupts of 8085 with their vector addresses. List them according to their priority. Explain maskable and non-maskable interrupts.

O2006

1) Draw a neat labeled diagram of generic ALU and explain its working.
2) What are hardware and software interrupts? List them with vector addresses.

M2007

1) Explain the interrupt system of Intel 8085 microprocessor.

O2007

1) Draw the block diagram of microcomputer and state the function of each block in brief.
2) What do you meant by 'Interrupt'. Write a short note on hardware interrupt and software interrupts.

M2008

1) What is the function of the following units in 8085 microprocessor:
   a) Program Counter b) Stack Pointer c) Incrementer/Decrementer
   d) General Purpose Register
2) Write a short note on flag register of 8085 microprocessor. Explain the significance of flag bits with one example.

Introduction to Microprocessor & organisation of 8085 microprocessor	
Mar-16	Explain the following: i) Accumulator ii) Program Counter iii) Stack Pointer
Oct-11	Give the functions of following pins: i) HOLD ii) CLKOUT iii) IO /
Mar-11	Define the following terms with suitable diagram: i) T-State ii) Machine Cycle iii) Instruction Cycle
Mar-17	Define the following terms with suitable diagrams : i) T-State ii) Machine Cycle iii) Instruction Cycle
Mar-10	Define the followings : i) T-State ii) Machine Cycle iii) Instruction Cycle
Mar-18	Define the terms- Machine Cycle, Instruction Cycle and T-State with a timing diagram.
Aug-18	Define: i) T-State ii) Machine Cycle iii) Instruction Cycle.
Jul-16	Describe in brief function of following pins in 8085 Microprocessor : i) ii) SOD iii) ALE

Oct-15	Describe in brief function of following pins in 8085 Microprocessor : i) READY ii) CLKOUT iii) $IO/\overline{M}$
Mar-12	Describe in brief the function of the following pins of 8085 Microprocessor: 3 i) $\overline{RD}$ ii) $\overline{WR}$ iii) ALE
Oct-10	Describe in brief the functions of the following pins of 8085 Microprocessor : i) S0 ii) S1 iii) IO/ to decide various operations
Mar-13	Describe in brief the functions of the following pins of 8085 microprocessor: i) IO / ii) SID iii) HLDA
Oct-14	Describe the functions of following pins of 8085: i) SID ii) READY iii) ALE
Mar-10	Describe the functions of the following pins of 8085 Microprocessor : i) X1 & X2 ii) AD0 to AD7 iii) A8 to A15
Oct-12	Differentiate between maskable and non maskable interrupts.
Mar-18	Draw a bit pattern of flag register of Intel 8085 and write the functions of any four flags.
Aug-18	Draw a labeled block diagram of 8085 Microprocessor.
Oct-12	Draw a labeled functional block diagram of microprocessor 8085.
Jul-16	Draw a neat labeled block diagram of 8085 Microprocessor.
Jul-16	Draw a well labeled block diagram of a generic microprocessor.
Aug-18	Draw and explain functional block diagram of ALU.
Jul-17	Draw and explain programming model of Intel 8085 Microprocessor.
Mar-13	Draw block diagram of 8085 microprocessor.
Mar-15	Draw block diagram of Generic Microprocessor.
Mar-10	Draw block diagram of the Microprocessor 8085.
Oct-10	Draw neat simplified block of CPU Architecture of Microcomputer.
Mar-18	Draw the functional block diagram of Intel 8085.
Mar-16	Draw the labeled internal block diagram of 8085 Microprocessor.
Oct-11	Draw the pin diagram of Microprocessor 8085.
Aug-18	Explain 16-bit Registers used in 8085 Microprocessor.
Mar-14	Explain all the Generations of Microprocessors and give example of each.
Mar-11	Explain ALU of generic microprocessor.
Mar-15	Explain any four flags of 8085 giving example.
Mar-12	Explain any three primary functions of the CPU of a Microcomputer.
Mar-11	Explain flag register of 8085 microprocessor with example.
Mar-14	Explain following flags of 8085 MPU: i) parity flag ii) carry flag iii) auxiliary carry flag
Aug-18	Explain following pins of 8085 Microprocessor : i) INTR ii) HOLD iii) HLDA
Oct-12	Explain following pins of 8085 Microprocessor. i) CLKOUT ii) $\overline{RD}$` iii) RST 5.5
Aug-18	Explain following unit of 8085 Microprocessor : i) Temporary Register ii) Serial I/O Control iii) Interrupt Control

Oct-10	Explain function of ALU with a simple block diagram.
Mar-14	Explain function of register A of 8085 MPU.
Mar-11	Explain function of the following pin in 8085 Microprocessor: i) HOLD ii) READY iii) $\overline{WR}$
Mar-14	Explain function of the following pins of 8085 MPU : i) HOLD ii) SID iii) READY iv)
Mar-15	Explain function of the following pins of 8085: i) $\overline{RD}$ ii) $IO/\overline{M}$ iii) $\overline{INTA}$
Oct-13	Explain functions of 8085 Microprocessor pins : i) RESETOUT ii) ALE iii) TRAP
Mar-13	Explain functions of following registers of 8085 microprocessor : i) Accumulator ii) Flag iii) Program Counter
Mar-10	Explain functions of following registers: i) Instruction register ii) Instruction Decoder iii) Temporary register
Jul-17	Explain functions of the following pins of 8085 Microprocessor: i) Multiplexed address/data bus pin (AD0-AD7). ii) RST 6.5 iii) CLK (OUT)
Mar-17	Explain functions of the following pins of 8085 Microprocessor: i) Multiplexed address/data bus pin (AD0-AD7). ii) RST 6.5 iii) CLK (OUT)
Oct-10	Explain hardware interrupts of 8085 microprocessor with their priorities and vector addresses.
Jul-17	Explain I/O mapped I/O scheme in 8085 microprocessor.
Oct-15	Explain in brief any three situations when multiplexing is useful for Data Transmission.
Mar-10	Explain in brief functions of the following registers in 8085 : i) Program counter ii) Stack Pointer iii) Accumulator
Oct-10	Explain in brief the functions of the following units of 8085 Microprocessor: i) Stack Pointer ii) General Purpose Registers iii) Program Counter iv) Instruction Register & Decoder
Mar-15	Explain Multiplexed Address and Data Bus of 8085 MPU.
Oct-14	Explain the following instructions in 8085 with example. i) RIM ii) SIM
Mar-11	Explain the following registers of 8085 Microprocessor: i) Stack Pointer ii) Program Counter iii) Instruction Register
Mar-15	Explain the following: i) T-State ii) Machine Cycle iii) Instruction Cycle iv) Fetch Cycle
Mar-18	Explain the function of ALU with a simple block diagram.
Mar-16	Explain the function of following pins of 8085 : i) HLDA ii) SID iii) READY
Jul-17	Explain the function of following pins of Intel 8085 : i) SOD ii) READY iii) HLDA
Mar-18	Explain the function of following pins on Intel 8085 : i) ii) iii)
Jul-16	Explain the function of following units in 8085 Microprocessor : i) Instruction decoder ii) Increment-Decrement address Latch iii) ALU

Oct-15	Explain the function of the following registers in 8085 Microprocessor : i) Stack Pointer ii) Instruction Register iii) Program Counter
Oct-15	Explain the terms in a Micro-Computer : i) Address Bus ii) Data Bus iii) Control Bus
Mar-12	Explain use of extended register pairs BC and HL of 8085 Microprocessor as pointers with the help of suitable examples.
Oct-12	Explain various operations performed by the status signals S0 and S1 & IO/ $\overline{M}$
Jul-17	Flag register contains data D5H. Interprte its meaning.
Mar-14	Give functions of the following 8085 registers : i) PC ii) SP iii) IR
Mar-12	In case of a Microprocessor Architecture, explain the following terms in brief : i) Address bus ii) Data bus iii) Control bus
Mar-10	List flags in 8085 and explain how they can be set or reset.
Oct-15	State the conditions of IO/ $\overline{M}$, S0 and S1 signals of 8085 Microprocessor for the following operations : i) Memory Read ii) I/O Write iii) I/O Read
Jul-16	The flag register 0f 8085 Microprocessor contains data D9H. Interprets it's Meaning.
Mar-13	The flag register of 8085 microprocessor contains the data AAH. Interpret its meaning.
Mar-14	What are interrupts? Explain maskable and non maskable interrupts of 8085 giving example of each.
Mar-15	What are the hardware interrupts? Explain vectored and non vectored Interrupts of 8085 MPU.
Mar-12	What are vectored interrupts? What are maskable and non maskable interrupts? State all hardware interrupts of 8085 Microprocessor with their priorities and branching or vector addresses.
Mar-18	What do you mean by Interrupt? List all software interrupts of Intel 8085.
Jul-16	What do you mean by vectored interrupt? List all hardware interrupts of 8085 microprocessor according to their priority order. Which of them is non maskable?
Jul-17	What is an Interrupt? List any four hardware Interrupts of Intel 8085 with their vector addresses.
Oct-11	What is flag? Explain flags in 8085 with diagram.
Oct-13	What is Interrupt? Differentiate between hardware and software interrupt.
Oct-14	What is interrupt? Explain software and hardware interrupt in 8085.
Oct-11	What is interrupt? List them according to order of priority also mention maskable and non maskable from these.
Oct-14	What is multiplexed address/data bus in 8085? Give its advantages.
Oct-14	What is stack? Give its related instructions in 8085.
Oct-15	What is T-State? Explain the three steps in execution of an instruction in Microprocessor.
Mar-17	What is vectored interrupt? State all hardware interrupts with their vectored addresses. Write the priorities of hardware interrupts.
Mar-16	What is vectored interrupt? State the different hardware interrupts with their priorities and branching addresses.

Mar-17	Write a function of following functional units of 8085 Microprocessor : i) Instruction Decoder ii) General Purpose Register iii) Data/Address Buffer iv) Status Register
Oct-13	Write a short note on evolution of Microprocessor giving one example of each generation.
Oct-14	Write a short note on evolution of microprocessor.
Mar-13	Write a short note on interrupts in 8085 microprocessor.
Mar-17	Write any three difference points between Memory Mapped I/O and I/O Mapped I/O addressing scheme.
Jul-17	Write any three primary functions of Microprocessor.
Oct-11	Write down the functions of an accumulator.
Oct-11	Write down the primary functions of microprocessor.
Oct-15	Write the functions of following units in 8085 Microprocessor : i) ALU ii) Timing and Control iii) Serial I/O control iv) Instruction Register and Decoder
Mar-17	What is microprocessor? List its functions.

Instruction to Intel X86 family	
Aug-18	Explain 16-bit version of X-86 family programming model with suitable diagram.
Oct-11	Compare 80486 and 80586.
Mar-12	Compare any four attributes of 486 DX with Pentium Processor.
Oct-12	Compare any four attributes of 80386 and Pentium processor.
Jul-16	Compare any four attributes of 8086 and 486 DX microprocessor.
Mar-13	Compare any four attributes of 8286 and 80486 processors.
Mar-17	Compare any three attributes of 80386 and 80486 Microprocessor.
Aug-18	Compare Intel 80286 Microprocessor with Intel 80486.
Aug-18	Compare Intel 80386 with Intel 80486.
Mar-16	Discuss in brief the members of X-86 family beginning from 80386 and upwards.
Oct-13	Draw and explain programming model of 32 bit version of X 86 Family.
Jul-17	Draw and explain the programming model of 16-bit version of Intel X86 Microprocessor family.
Mar-14	Draw programming models of X86 16 bit and X86 32 bit Microprocessor.
Mar-16	Draw the labeled diagram of X-86 family flag register.
Mar-10	Explain 'Dual Pipeline' and 'Branch Prediction' features of Pentium.
Mar-13	Explain advantages of the following features of the Pentium Processor : i) Dual Pipelining ii) On Chip Caches iii) Branch Prediction iv) 64bit Data Bus
Mar-18	Explain any three important features of Pentium processor.
Mar-16	Explain in brief programming model of X-86 Family.
Mar-11	Explain main features of a Pentium Processor.
Mar-10	Explain programming model of 16bit version of X86 family.
Mar-16	Explain the advantages of following features of Pentium Processor : i) Dual-Pipelining ii) Prefetching iii) Branch Prediction iv) Internal Data Bus
Oct-15	Explain the advantages of the following functions of the Pentium Processor: i) Dual Pipelining ii) On Chip Caches iii) Brach Prediction iv) 64-bit Data Bus
Oct-10	Explain the following features of Pentium Processor: i) Dual Pipelining ii) Branch Prediction iii) On Chip Cache iv) 64 bit Data bus

Oct-11	Explain X86 flag register with diagram.
Mar-15	State any three features of Pentium Processor.
Oct-14	Write a note on Pentium.

Chap 7 Introduction to Intel X-86 Family

H.S.C. BOARD TOPIC WEIGHTAGE : 4 MARKS

4 Mark Que = 1 = 4x1 = 04

The microprocessors are evaluated from 4-bit To 32-bits. In 4-bit microprocessor the word length is very minimum as compared to 32-bit microprocessor i.e. each time of evolution the microprocessor's word length are doubles. In each evolution the architectures of microprocessor is also changed.

The 8085 microprocessor is a 3rd generation 8-bit microprocessor & 8086 is extended version of 8085. It is a 4th generation 16-bit microprocessor. So generally these microprocessor are known as advance microprocessor.

features of 8086 microprocessor over 8085 microprocessor :

1) Very powerful computing devices. So process speed is increased.
2) In today's PC these microprocessor are generally found because it has higher operating speed, instruction cache memory, higher word-size etc.
3) The 8086 microprocessor also supports to the numeric Co-Processors.
4) It has separate CPU.
5) It performs an arithmetic functions such as add, subtract, multiply, divide & trigonometric functions.
6) It returns results much faster than general CPU.
7) The general CPU may be engaged in performing other functions while Co-Processor is working.

Disadvantages of 8086 microprocessor :

1) It requires sophisticated O / S & application S / W.
2) These have very complex system & installation of this microprocessor is very hard.
3) These requires multi-user & multi –tasking applications.

X-86 family OR X-86 microprocessor :

The following are the major families of X-86 microprocessors which has different attributes & different operating features:

1) Features 8088 processor :

a) It contains 8 bits Data Bus & 20 bits Address Bus INTEL introduces it at 1978.
b) This microprocessor operates at min 5 to max 8 MHz speed.
c) It contains External 8087 as math-coprocessor & External Unit as Memory Mgt.
d) It contains 1 MB Physical Memory Addressed & 16-bits Internal data word size.

2) Features 8086 processor :

a) It contains 16 bits Data Bus & 20 bits Address Bus INTEL introduces it at 1978.
b) This microprocessor operates at min 5 to max 10 MHz speed.
c) It contains External 8087 as math-coprocessor & External Unit as Memory Mgt.
d) It contains 1 MB Physical Memory Addressed & 16-bits Internal data word size.

3) **Features 80286 processor :**

a) It contains 16 bits Data Bus & 24 bits Address Bus IBM introduces it at 1982.

b) This microprocessor operates at min 6 to max 20 MHz speed.

c) It contains External 80287 as math-coprocessor & Internal MMU as Memory Mgt.

d) It contains 16 MB Physical Memory Addressed & 16-bits Internal data word size.

4) **Features 80386 processors :**

This is a extended version of 80286 processor. So generally this is called as logical extension of 80286. This provides high operating speed & high MMU so approximately the speed is increased. It has 2 version development 386 S-X & 386 DX the only difference in Data Bus length 386 S-X contains 16-bit data bus where as 386 D-X contains 32-bit data bus. The instruction cache memory is also higher in 386 D-X it approximately doubles i.e. 386 S-X contains 16 bytes instruction cache memory where as 386 D-X contains 32 bytes instruction cache memory. The 386 S-X contains Eternal 80287 math coprocessor so arithmetic manipulation speed is lower than 386 D-X it uses External 80387.

a) It contains 32 bits Data Bus & 32 bits Address Bus INTEL introduces it at 1985.

b) This microprocessor operates at min 16 to max 50 MHz speed.

c) It contains External 80287 & 80387 math coprocessor (only found in 386-DX) & it contains Internal MMU as Memory Mgt.

d) It contains 4GB Physical Memory Addressed & 16-bits-32 bits Internal data word size.

e) It contains 16 bytes Instruction Cache memory & 256 bytes Data Cache memory.

5) **80486 processors :**

This is a extended version of 80386 processor. So generally this is called as logical extension of 80386. This provides high operating speed & high MMU so approximately the speed is increased. It has 2 version development 486 S-X & 486 DX the only difference in math coprocessor used in 486-SX External 80387 is used where as in 486 D-X Internal math coprocessors are used.

a) It contains 32 bits Data Bus & 32 bits Address Bus INTEL introduces it at 1989 (486 S-X) & at 1991 (486 D-X) is introduced .

b) This microprocessor operates at min 25 to max 50 MHz speed.

c) It contains External 80387(in 486 S-X) & Internal math coprocessor (only found in 486-DX) & it contains Internal MMU as Memory Mgt.

d) It contains 4GB Physical Memory Addressed & 32 bits Internal data word size.

e) It contains 32 bytes Instruction Cache memory & 8 KB Data Cache memory.

6) **Features 80586 processors OR Pentium Processors:**

This is a extended version of 80486 processor. So generally this is called as logical extension of 80486. It provides high processing speed because in this version dual pipelining is found in data bus & address bus architecture. It contains on-chip caches so that this facility improves speed of Pentium processor. It also capable for deciding states because it contains branch prediction feature using this it guesses where next instruction following conditional instruction or not. The data transfer speed is comparatively higher than all processors because it has 64-bit data bus so it doubles the data bus. It transfers data by twice with 32-bit sizes.

a) It contains 64 bits Data Bus & 32 bits Address Bus INTEL introduces it at 1993.
The data bus & address bus uses super scalar architecture which incorporates a dual-pipe lined processor. So that this buses is capable for executing more than one instruction per clock cycle.

b) This microprocessor operates at min 50 to max 100 MHz speed.

c) It contains Internal Math Co-processor. So inbuilt manipulation is done. It also contains Internal MMU as memory management.

d) It contains 4GB Physical Memory Addressed & 32 bits Internal data word size.

e) It contains 32 bytes Instruction Cache memory & 8 KB Data Cache memory.

**** Advance Features of Pentium microprocessor OR Advantages of Pentium microprocessor**

1) **Branch Prediction :-**

A new advanced computing technique is used in Pentium is called the branch prediction, the Pentium makes an educated guess where the next instruction following a conditional instruction will be. This prevents instruction cache from running dry during conditional instructions.

2) **On Chip caches :-**

It has on-chip-caches. So that the data & code on-chip caches improves the processing speed of the Pentium processor.

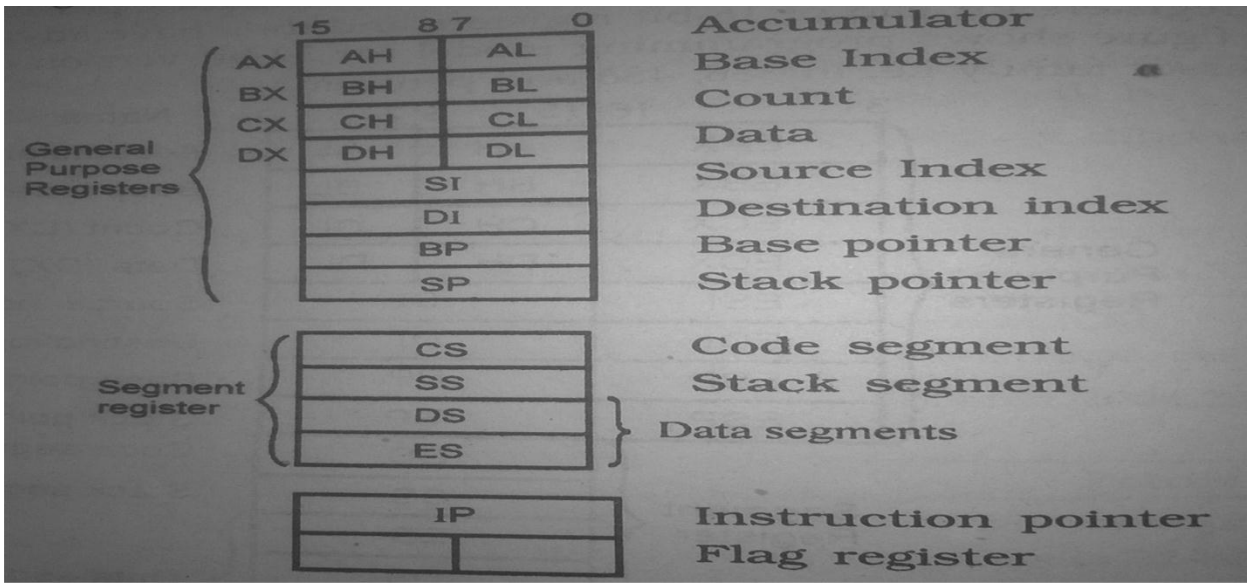
3) **Dual Pipelining :-**

A Pentium processor used a super scalar architecture which incorporates a dual-pipelining. Using this facility the Pentium processor increases the speed of instruction processing per clock cycle. The dual-pipelining has capable for performing more than one task so it very useful in multitasking environment.

4) **64 bit data bus :-**

It allows higher speed of data transfer to it. The data transfer spped of Pentium is twice as fast as processor with 32 bit data bus.

** Programming Model of 16-bit version of X-86 Family :



The 8088 & 8086 defines the basic programming model for X-86 family. The 16-bit version of programming model is used in 16-bit microprocessors of X-86 family i.e. in 8086, 80286 & 80386. The programming model can have different register sections as illustrated in following figure :

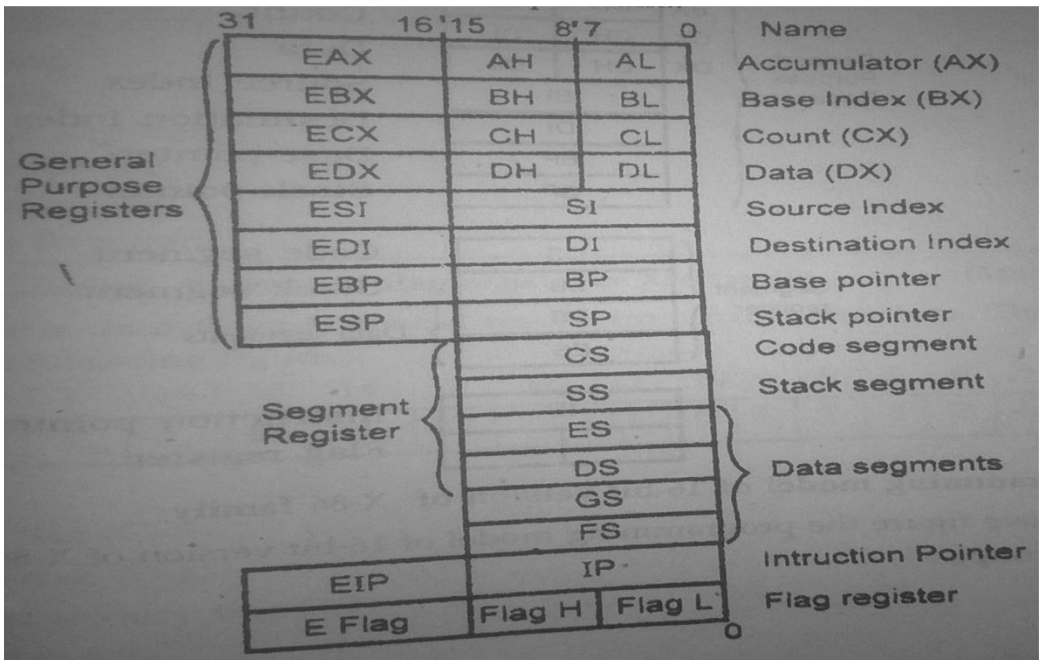
In fig it is illustrates that the programming model of 16-bit version of X-86 family consists of three register groups. Such as general purpose registers, Segment registers & instruction pointer flag register section.

a) General Purpose Register Section : These are collection of register. In this section all register are 8-bit registers which are paired in higher order & loser order. So combining of higher & lower they forms 16-bit register. So that the full 16-bit registers are referred as AX, BX, CX & DX where " X " stands for extended. In above general purpose register section we seen that the " L " indicates the lower byte & " H " indicates the higher byte. The register SI, DI, BP & SP is also treated like 16-bit special purpose registers. These are pointer registers because SI register points to Source index location, DI points to Destination Index location, BP points to Base memory location & SP points to the Stack-Memory location.

b) Segment Register Section : These are collection of CS (Code Segment), SS (Stack Segment), DS (Data segment) & ES (Data Segment). All these register manages operation with external memory. It also performs address computations & data movements.

c) Instruction Pointer (IP) & Flag registers : These are always 16-bit register. The instruction pointer helps to goes next memory location that means every next instruction is reads by instruction pointer. The flag register is status information of desired results that means dependent of an accumulator result these are set or resets. It flags has special task & special meaning.

** Programming Model of 32-bit version of X-86 Family :



The 8088 & 8086 defines the basic programming model for X-86 family of advanced microprocessor. It introduced a newer advanced version of 16-bit X-86 family which is called as extended version of x-86 family is 32-bit version of X-86 family. These versions have a greater computing power because they are faster & advanced version addressing techniques. It uses 32-bit version instead of 16-bit register. The programming model can have different register sections as illustrated in following figure :

In fig it is illustrates that the programming model of 32-bit version of X-86 family consists of three register groups. Such as general purpose registers, Segment registers & instruction pointer flag register section.

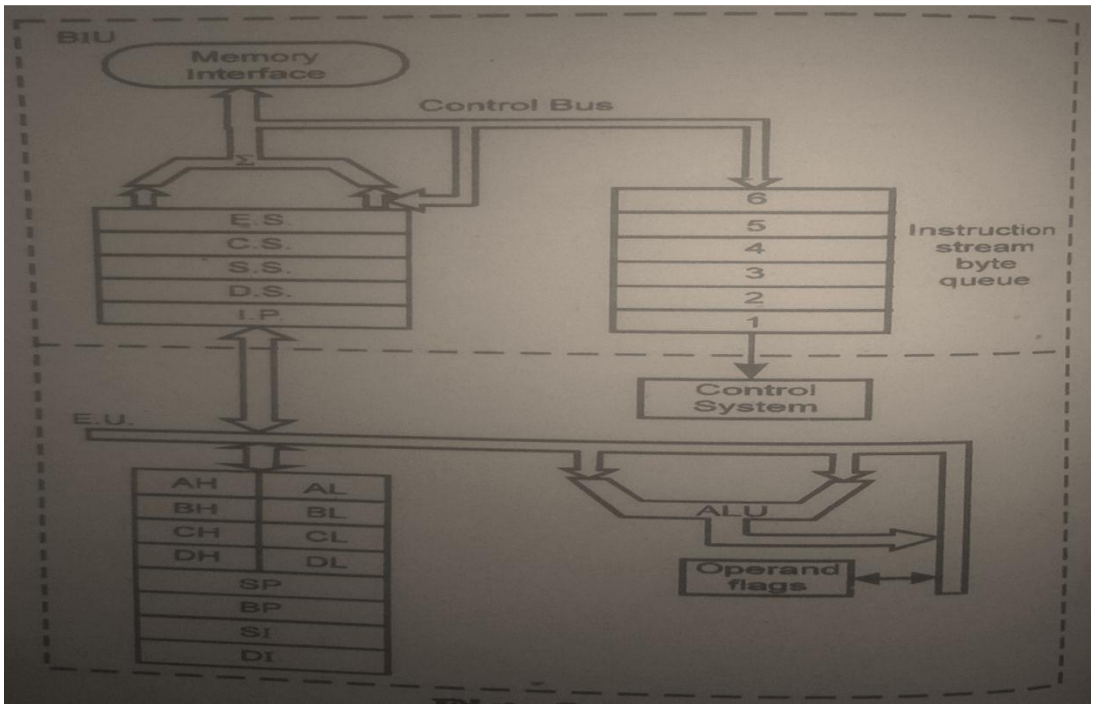
a) General Purpose Register Section : These are collection of register. In this section all register are 8-bit registers which are paired in higher order & loser order. So combining of higher & lower they forms 16-bit register. So that the full 16-bit registers are referred as AX, BX, CX & DX where " X " stands for extended. In above general purpose register section we seen that the " L " indicates the lower byte & " H " indicates the higher byte. The register SI, DI, BP & SP is also treated like 16-bit special purpose registers. These are pointer registers because SI register points to Source index location, DI points to Destination Index location, BP points to Base memory location & SP points to the Stack-Memory location.

In fig it is also illustrates that 32-bit is a advanced version or extended version of 16-bit of X-86. So that remaining 16-bit are known as extended version facility it has 16-bit advanced eight different types of general purpose register such as EAX, EBX, ECX,EDX, ESI, ESP & EBP registers. Where " E " tells that these registers have extended length. Each register can addressed in 1,8,16 & 32 bit models. These registers are stores data during computations.

b) Segment Registers : The second group of 32-bit version is segment register. This group consists code segment (CS), stack Segment (SS), & four data segments registers such as DS, ES, FS & GS. These all registers are 16-bit special purpose registers. These registers manages operation with eternal memory. It also performs address computation & data movements.

c) **Instruction Pointer (IP) & Flag registers :** These are always 16-bit register. The instruction pointer helps to goes next memory location that means every next instruction is reads by instruction pointer. The flag register is status information of desired results that means dependent of an accumulator result these are set or resets. It flags has special task & special meaning.

** Architectural Block Diagram of 8086 microprocessor



The 8086 CPU is divided into two independent functional parts such as :

1) Bus Interface Unit (B. I. U.)
2) Execution Unit (E. U.)

1) Bus Interface Unit : This is interacted to data bus & address bus. So this B.I.U. of 8086 CPU sends addresses, fetches instructions from memory, reads data from ports/ memory & writes data to ports/ memory. In other words this section handles the transfer of data & address on buses for execution unit. It consists of following parts :

a) Queue : To speed up execution of program, B.I.U. fetches six (6) instructions bytes ahead of time from memory & stores them for E.U. in the FIFO (First In First Out) register called as queue.

b) Segment Register : These register contains code segments, stack segments & two data segments such as data segment & extra segment. These register manages operation with external memory. Address computations & data movements are performed here, Thus this registers stores 16-bit starting address of memory segment from which BIU is fetching instructions code bytes.

c) Instruction-Pointer : This register holds 16-bit address of next code byte within code segment, then it transfers data to execution unit after performing task from Execution Unit then next instruction address is also hold by Instruction Pointer so again control goes to there.

2) Execution Unit : This unit tells B.I.U. where to fetch instruction or data , it also decodes instruction & executes them.

Functional Parts of Execution Unit :

The following are the functional parts of execution unit of 8086 microprocessor :

a) Flag Register : These are flip-flop. These are sets & resets according to conditions. These are affected on the results stored at accumulator. 8086 contains 16-bits flag register with nine (9) active flags & remaining are undefined.

b) Accumulator : It is used for all arithmetic & logical manipulation. The final results are also stored in accumulator. It is a 8-bit register & it contains higher order byte as well as lower-order byte.

c) General Purpose Registers : These are 8-bit registers. Generally available for user. 8086 has eight different types of GPR. These registers can be used individually for temporary storage of 8-bit data. " H " indicates the higher byte as well as " L" indicates lower byte & full 16 bit registers are referred as AX, BX, CX & DX. Where "X" stands for extended.

d) Stack Pointer : These are 16-bit register. These are pointer-register because these are generally used for to points the stack locations within a segment. This is interacted to upper most toppers memory.

e) Base Pointer (B.P.) : These are 16-bit register. These are pointer-register because these are generally used for to points the base memory locations within a segments.

f) Destination Index (D. I.) : These are 16-bit register. These are pointer register because these register are generally used to points the destination memory location.

h) Source Index (S. I) : These are 16-bit register. These are pointer register because these register are generally used to points the source memory location

Q) **What are advance features of X-86 Microprocessor family? Draw and explain X-86 family falg register.**

Advance features of X-86 microprocessor family are as follows :

1) It is capable of performing various computing functions and making decisions to change the sequence of program execution.
2) It is very powerful computing device.
3) Coprocessor :- The advanced microprocessors are supported by numeric coprocessor. It is separate CPU which performs arithmetic functions and trigonometric functions.
4) Operating System : - Microprocessor works with multiuser and multitasking operating system.
5) Virtual Memory :- Advanced microprocessor supports virtual memory technique for storing large volume of data.

6) Microprocessor includes special instructions and internal h/w which allows a programmer ot to write s/w without knowing how much memory is available.

** X86 Flag register :-

1) The flag register of X86 family is 32 bit.
2) In which 8085 microprocessor has 8 bit flag register from bit 0 to 7 with 5 active flags.
3) 8086/8088 microprocessor is 16 bit microprocessor. It contains 0 to 11 flags i.e. 8085 flags and 8086 new flags. It contains 9 active flags from bit 0 to 11 out of this 5 flags are of 8085 microprocessor and remaining of 8086 new flags.
4) 80286 has also 16 bit flag register but 12 to 14 bits are added. It contains 12 active flags from bit 0 to 14.
5) 80386 microprocessor has 32 bit register. It contains 16 and 17 bits were introduced. It is from bit 0 to 17. It contains 13 active flags.
6) 80486 has 32 bit flag register. It contains new 18^{th} bit flag. Remaining from 19 to 31 bits are don't care flags or reserved flags. It contains 14 active flags.

Flag diagram of X86 family

31 ……..18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	A_c	V_M	R_F	O	N_T	IO	PL	O	D	I	T	S	Z	X	AC	X	P	X	CY

Where 1) CY : Carry flag 2) P : Parity flag 3) AC : Auxiliary carry flag
4) Z : Zero flag 5) S : Sign flag 6) T : Trap flag
7) I : Interrupt flag 8) D: String Direction flag
9) O : Overflow flag 10) IOPL : I/O Privilege level
11) N_T : Nested task flag 12) R_T : Resume flag
13) V_M : Virtual mode flag 14) A_c : Alignment check flag

Instruction to Microcontroller	
Mar-12	Compare 8052 Microcontroller with 8051 Microcontroller.
Oct-14	Compare between Microcontroller 8051 and 8052.
Aug-18	Compare Microcontroller 8051 with 8052.
Oct-13	Define Microcontroller and state its advantages over Microprocessor based System.
Oct-12	Define Microcontroller. State any four features of 8051 Microcontroller.
Mar-16	Differentiate between Micro-controller and a Micro-processor.
Mar-11	Differentiate between Microcontrollers 8051 and 8052.
Mar-16	Discuss the Micro-Controllers in 8051 family.
Oct-10	Draw a neat block diagram of 8051 Microcontroller.
Mar-14	Draw and explain complete memory map of 8051 Microcontroller.
Mar-16	Draw the memory register map of Micro-Controller 8051.
Oct-14	Explain memory map in microcontroller 8051 with neat diagram.
Oct-13	Explain memory map of 8051.
Jul-17	Explain memory map of Intel 8051 Microcontroller with help of diagram.
Mar-13	Explain various applications of microcontroller.
Mar-12	Give any eight important features of 8051 Microcontroller.
Oct-12	List any three Microcontrollers of 8051 family and state one feature of each(other than 8051).
Oct-11	List the features of Microcontroller 8051.
Mar-11	State any eight features of Microcontroller 8051.
Oct-12	State any four advantages and four applications of mircrocontroller 8051.
Oct-15	State any six applications of a Microcontroller.
Mar-15	State any six applications of Microcontroller.
Mar-15	State any six features of 8051 Microcontroller.
Oct-13	State any three features and applications of 8051 Microcontroller.
Mar-11	State RAM and ROM size of the following Microcontrollers : i) 8048 ii) 8049 iii) 8050
Oct-10	What is a Microcontroller? State any four advantages of Microcontroller over Microprocessor.
Oct-15	What is a Microcontroller? State any six features of 8051 Microcontroller.
Mar-15	What is a Single Chip Computer? State its advantages.
Mar-10	What is Microcontroller? Discuss members of the Microcontroller 8051.
Jul-16	What is Microcontroller? State any six application of a microcontroller.
Mar-18	What is Microcontroller? State any six important features of Intel 8051 Microcontroller.
Mar-17	What is Microcontroller? State any three advanced features of 8052 Microcontroller over 8051 Microcontroller.
Mar-14	What is Microcontroller? State any two advantages over MPU based system.
Jul-16	With suitable block diagram explain memory register map of 8051 microcontroller.
Oct-11	Write a short note on Microcontroller 8051 family.
Jul-17	Write any six applications of Microcontroller.
Mar-17	Write any two features of following Microcontrollers : i) 8048 ii) 8052 iii) 8031 iv) 8050
Mar-10	Write down the applications of Microcontroller.
Mar-18	Write the RAM and ROM size of 8048, 8049 and 8050 Microcontrollers.

Chap-8 Introduction to Microcontroller

Q1) What is Microcontroller? Explain the various applications of microcontroller?

Def: " A microcontroller is a complete microprocessor system, consisting of microprocessor, limited amount of ROM, RAM and parallel I/O port, built on a single integrated circuit"

Applications of microcontroller:----(

The microcontroller provides following different applications :

1) A home security system, a tape deck and intelligent multimeter can be builds by using microcontroller
2) A PC keyboard are implemented with a microcontroller. It replaces scanning, denouncing, matrix decoding and serial transmission circuit.
3) Microcontroller is a single chip microcomputer. So they are used in medical instruments.
4) Many low cost products such as electronic toys, electric drills, microwave ovens, VCRs are based on microcontroller.
5) Microcontroller are used as a independent controllers in machines or as a slaves in distributed processing.
6) Microcontrollers are used as a machine tools, chemical processors and sophisticated guidance control.

Q2) What are advantages of microcontroller same over the microprocessor based system?

The following are advantages of microcontroller same over the microprocessor based system:

1) The cost of microcontroller is less than a microprocessor based system.
2) A microcontroller has more I/O components than a microprocessor based system.
3) Microcontrollers can be used in wide variety of intelligent products such as in PC keyboards. But the microprocessor based system cannot be used in such intelligent products.
4) Many low cost products such as electronic toys, electric drills, microwave ovens, VCRs are based on microcontrollers. This is not the case with microprocessor based system.

Q3) Compare with 8051(microcontroller) and 8085 microprocessor?

Microprocessor	Microcontroller
1) Normally connected with I/O devices & external memory	1) It is single chip microprocessor with built-in-circuits
2) Microprocessor based system is costly	2) Microcontroller based system us a low-cost system
3) ex: MPU 8085, 8086, 80486 etc	3) ex: Microcontroller such as 8048 family processors, 8051 family processor
4) Used as CPU of PC	4) Used as controller of small mechanism.

Q4) Write a short note on complete microprocessor based system?

OR What is microcontroller? Discuss in brief?

1) A microcontroller is a complete microprocessor based system consisting of microprocessor, limited amount of ROM or EPROM, RAM and I/O ports built on a single integrated circuit.
2) Microcontroller is in fact a microcomputer but it is called so because it is used to perform controlled functions.
3) The designer of a microcontroller identify all the needs to build a simple microprocessor system and puts as many as possible in a single IC.
4) The microcontroller must include full or nearly full implementation of standard microprocessor, ROM or EPROM, RAM, Parallel I/O ports, timer, a clock, serial ports etc.
5) A microcontroller is more complex than a microprocessor because it consists of many I/O components. e.g. Intel's 8048 microcontroller (1st generation) and Intel's 8051 microcontroller (2nd generation)

Q5) What are features provide by first generation microcontroller OR 8048 microcontroller?

The main features of 8048 microcontroller as listed below:

1) 8048 microcontroller has clock having frequency 2MHz to 4MHz.
2) 8048 microcontroller has 27 I/O lines.
3) 8048 microcontroller has 1KB ROM or EPROM.
4) 8048 microcontroller has 64KB RAM.
5) 8048 microcontroller has one 8-bit timer-event counter.
6) Address capacity of 8048 microcontroller is 4KB.

Q6) What are main features provided by second generation microcontroller OR 8051microcontroller?

The main features of 8051 microcontroller is as listed below:

1) The 8051 microcontroller has an 8-bit ALU.
2) The 8051 microcontroller has 4KB i.e. 4KX8-bit ROM or EPROM.
3) The 8051 microcontroller has 128 bytes i.e. 128X8 bit RAM.
4) The 8051 microcontroller has dual 16-bit timer event counter.
5) The 8051 microcontroller has 32 I/O lines for four 8-bit I/O port.
6) The 8051 microcontroller has can addresses 64KB of program memory.
7) The 8051 microcontroller has powerful instruction set which contains 111 instructions.
8) The 8051 microcontroller has contains two external interrupts.
9) The 8051 microcontroller has clock speed upto 12 MHz.
10) The 8051 microcontroller has contains a full-featured serial port.

Q7) Draws an architectural block diagram of 8051 and explain it detail?

The 8051 is a second generation 8-bit microcontroller. The first 8-bit microcontroller was 8048. The 8051 microcontroller provides a significantly more powerful architecture, a more powerful instruction set and full featured serial port.

The fig is illustrated that the architectural block diagram for 8051 microcontroller. In fig. It is shown that the two connections internal connection and external connections.

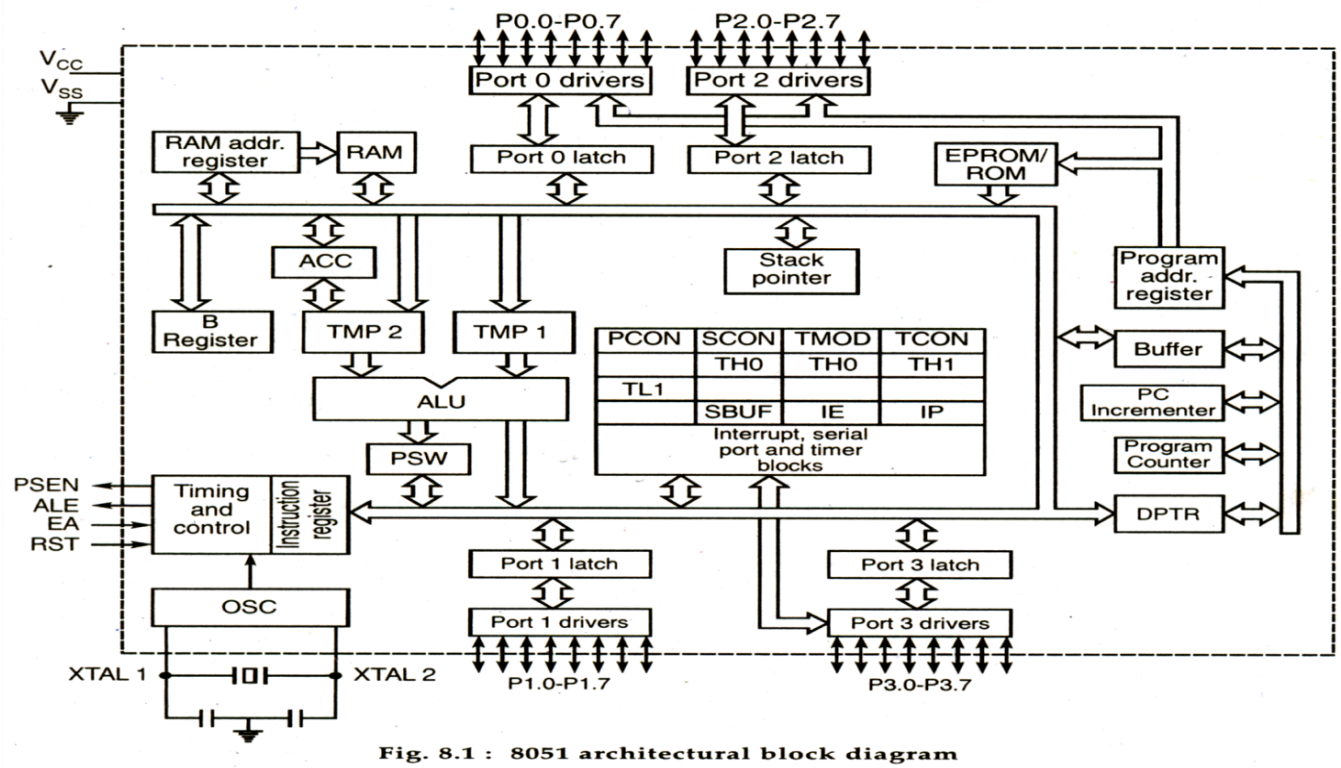


Fig. 8.1 : 8051 architectural block diagram

a) External view OR external connection :--(

An external connection is very simple. This needed 32-pins by four 8-bit bi-directional I/O ports. An 8 additional pins provides power which allows you to connects clock crystals and provides few timing & control signals.

b) Internal view OR internal connection: --→

An internal view of the 8051 microcontroller is very complex than external view. It consists of ALU, accumulator, stack pointer, a block registers and general purpose register such as B reg etc. All of these devices are connected to 8-bit internal data bus. Each I/O port is also connected to 8-bit internal data bus through a series of registers. These registers are hold data during I/O transfers and control I/O ports. In this view there are two memory modules such as RAM and ROM.

i) **RAM and ROM :-→** The internal view of 8051 has internal 4KROM and 128 bytes RAM. Which is used for storing the data temporary.

ii) **RAM address Register :-**(It holds the address bits of RAM.

iii) Accumulator :(After ALU performs its operation then processed result is stored into intermediate accumulator. It also holds the one i/p for ALU as operand during ALU operation.

iv) **TMP 1, TMP 2 and B-register :-**(These are general purpose registers. In which TMP 1 and TMP 2 are used as temporary registers during ALU operation it holds the operands intermediately it is given to ALU during operation that means the 2nd operand for operation of arithmetic and logical operation is stored into register or memory or immediate it is not directly gives its value during ALU operation so this is stored into TMP 1 and TMP 2. The register B is used as general purpose register which stores data.

v) **ALU : -**(It performs an arithmetic and logical operation by accepting i/p from ACC and TMP 1/TMP 2. After processing the processed result always transferred to an ACC. So that ALU is performs its operation association of ACC, TMP 1/TMP 2 and PSW. The content of PSW is depends upon whatever data in ACC.

vi) **PSW :** PSW stands for program status word or processor status word that means it shows the status operation performed in ALU. The status of PSW is ser or reset according to ALU operation. It contains different flags or flip-flop.

vii) **Stack pointer : -**(This is a 8-bit register in 8051 microcontroller. This is used in stack operation. It is a pointer register which points to stack addresses which resides topper most part of RAM address. The operation of stack is in LIFO manner.

viii) **DPTR :-**(This is a 16-bit register of 8051 microcontroller. It is a data pointer register. The 16-bit is made of DPTR is high order byte i.e. DPH (8-bit) and low order i.e. DPL (8-bit).

ix) **PCON :-**(It is a power control register. It is used to operates microprocessor in a special modes which conserve power until you wake up microprocessor.

x) **SCON :-**(**I**t is a serial port control register. This is a 8-bit register. It is used to tell serial port is how to operates.

xi) TMOD :-(It is a counter timer mode register. It is used to sets the mode of counter timers.

xii) **TCON :-**(It is counter-timer control register. The flags in this register either shows the status of the counter-timers or they are used to enables or disables counter-timer functions.

xiii) **Port 0 port and Port 0 driver, Port 1 port and Port 1 driver, Port 2 port and Port 2 driver, Port 3 port and Port 3 driver : -**(The 8051 microcontroller has contains four 8-bit bi-directional I/O ports such as port 0, port 1, port 2 and port 3. Each port has contains its own port latches for latching purpose such as port 0 latch, port 1 latch, port 2 latch and port 3 latch. This port latches allows to stores data going out of the port or coming into the port.

xiv) **SBUF: -(** It is a special function register. The 8051 serial interface is full-duplex serial port and SBUF register is used to transfers & receives data at the same time.

xv) **IE :-(I**t is an interrupt enable register. They are used to enable the interrupt.

xvi) **IP :-(I**t is interrupt priority interrupt register. This is used for controlling the priority of the interrupt of 8051 microcontroller.

xvii) **ALE : -(** This is an address latch enable signal. This is used as latch during multiplexed address/data bus. Therefore, this gives the information of line of multiplexed address/data bus.

xviii) **PSEN :-(** This is a control signal is used to reads the external program memory.

Q8) Explain 8051 memory mapping for 8051 microcontroller with the help of neat diagram?

The 8051 microcontroller has contains two types of separate memory spaces as below. This memory space is also shown in the memory mapping diagram:

a) Program Memory Space

b) Data Memory Space

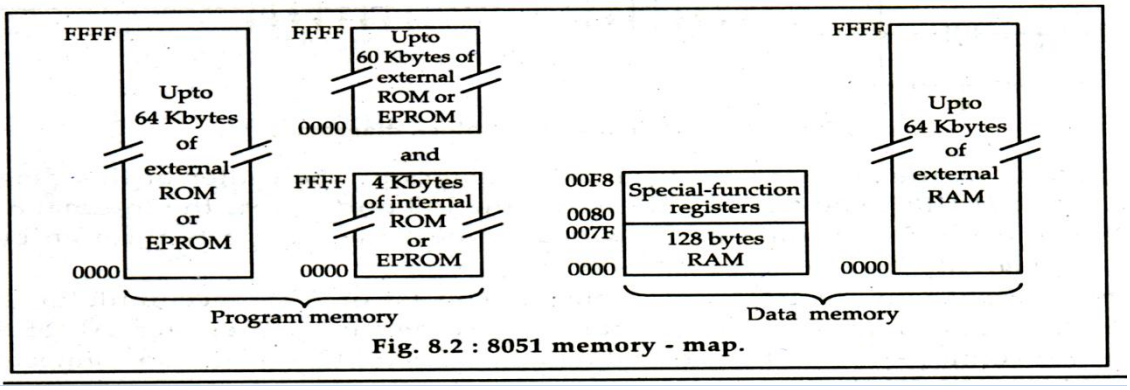


Fig. 8.2 : 8051 memory - map.

a) Program Memory Space :

1) The program memory space is read-only memory space i.e. ROM space.
2) This memory space is used for storing programs and variables data.
3) It is possible to reads program instructions from this space, but the processor cannot writes data into this memory space.
4) All instructions fetches are taken from program memory space.
5) The 4KB program memory can be expanded by an additional 60KB making it 64KB program memory.

b) Data Memory Space :-(

1) The data memory space is a read/write memory space.
2) The processor can reads data from this memory space and can writes data to this memory space.
3) It cannot executes instructions from this memory space. The 8051 microcontroller's internal RAM is in this memory space.
4) The 128 bytes of internal RAM provides general read/write data storage. Some part of this is often referred to as registers.
5) The 8051 microcontroller has 22 special function registers which are not part of 128 bytes of RAM. They occupy memory space from 80H to F8H. These registers are used for their intended purpose.
6) The data memory can also be expanded to 64KB

The 8051 microcontroller can also be operated with common memory. In this case, 8051 microcontroller only has 64KB of total external memory. In this configuration 8051 can inputs block of data through its serial communication port which loads that data in memory and then executes that data as a program. This mechanism is known as downloading program. It is a very common technique used to change the program operating in a remote microprocessor based controller.

Q9) Explain well labeled diagram of 8051 microcontrollers family of processors? Explain in detail other microcontrollers in 8051 microcontroller?

8051 is a second generation microcontroller. It contains other microcontroller with various features the microcontrollers included in 8051 microcontroller family such as follows:

a) 8048 b) 8049 c) 8050 d) 8052 e) 8031 f) 8032 g) 8052 AH-Basic

These all microcontrollers included 8051 family and provides various features as illustrated below:

a) <u>8048, 8049 and 8050 microcontrollers :-</u>(

1) Intel's first microcontroller was 8048. The 8048, 8049 and 8050 all have its own identical architectures with the exception of memory size.
2) In each case, the memory is doubles. The 8048 supports 1 KB of internal memory whereas 8049 supports 2 KB of internal memory and 8050 supports 4KB of internal memory..
3) 8048 has 64bytes internal RAM, including 32 bytes of register or memory locations. The 8049 and 8050 have a total of 128 and 256 bytes RAM respectively.
4) These microcontrollers are low cost products and hence are very popular.

b) <u>8052 microcontroller: --</u>(

1) 8052 is a simple expansion of 8051 microcontroller.
2) It has upto 8KB of onboard ROM and 256 bytes of onboard RAM.
3) 8052 allows programmers to write larger programs and that can use more data.
4) The cost of 8052 is more than that of 8051 microcontroller.
5) The 8052 also has one extra 16-bit counter-timer. This counter timer gives more flexibility.

c) <u>8031 and 8032 microcontrollers : --</u>(

1) The alternative version of 8051 and 8052 are 8031 and 8032.
2) These devices do not have any onboard ROM. It may use external ROM for program memory.
3) These are excellent devices for prototyping and low-volume products.

d) 8052 AH-Basic : --(

1) Another form of 8052 is 8052 AH-Basic. This is a special 8052 microcontroller which has BASIC programming language in ROM so name is 8052 AH-BASIC.
2) Using BASIC instructions a programmer can writes instructions for this 8052 rather than assembly language.

Chap 6 : Instruction set & Programming of 8085

H.S.C. Topic weightage : 43 Marks

1 Mark M.C.Q. = 1 = 1x1 = 01
3 Mark que = 4 = 3 x4 =12
5 Mark Assembly Language Program = 6 = 6x5 =30

Q1) What is instruction?

An instruction is a command given to microprocessor to perform a specified operation on given data.

Q2) What is instruction set?

The entire group of instructions is called as instruction set of microprocessor.

Q3) Why instruction set?

The programmer can write the program in assembly language using these instructions.

Q4) Explain two parts of instruction?

Each instruction of 8085 microprocessor consists of two parts i.e. opcode (operation code) and operand.

Opcode :

The first part of instruction which specifies the operation to be performed by the microprocessor is called as opcode.

Operand:

The second part of the instruction is the data to be operated on and it is called as operand.

Mnemonic: Are the meaningful words which defines operation performed by instruction during execution.

Q5) What are various techniques to specify operand?

There are various ways to specify data or operand for an instruction given below:

1) 8-bit or 16 bit data may be directly given in instruction itself.
e.g.1) MVI A, 02H; 2) LXI H, 2500H;

2) The address of memory location (16-bit) or I/O port address (8-bit) may be given in instruction itself.
e.g.1) STA 3500H; 2) IN 02H; 3) OUT 30H;

3) In some instruction only one register is specified. The content of the specified register is one of the operand. It is understood that the other operand is in the accumulator.
e.g. ADD B;

4) Some instruction specify one or two register. The contents of registers are the required data.
e.g.1) MOV A,B; 2) INR B

5) In some instruction data is not specified i.e. implied. The most instruction of this type operate on the content of accumulator.
e.g. CMA ;

Instruction Format OR Types :

Q6) How instruction of 8085 are classified?

Depending upon the size of machine codes or the instruction occupied in memory the 8085 microprocessor instructions are classified into three types as like below:

1) One Byte Instruction :

A 1byte instruction includes the opcode and the operand in the 8bits only i.e. one byte. It is also called as one word instruction.
Example MOV A,B

2) Two Byte Instruction :

In 2byte instruction the first byte is opcode and second byte is operand i.e. either 8-bit data or 8-bit address.
Example MVI A, 08H;

3) Three Byte Instruction :

In 3byte instruction the first by te is opecode and second and third byte bytes are operands i.e. 16-bit data or 16-bit address.
Example 1) LXI H, 3400H; 2) STA 3200H;

Q7) What is addressing mode? How they are classified?

Addressing Mode :

The various ways of specifying data or operands for instructions are called as addressing modes.

Classification of Addressing Mode:

The 8085 addressing modes are classified into following types:

1) Register Addressing Mode :

In register addressing mode the source and destination operands are in the general purpose registers. The opcode specifies the operation and registers to be used to perform the operation.

Example: MOV A, B;

2) Direct Addressing Mode :

In direct addressing mode the address i.e. 8-bit or 16bit of the operand or data is given in the instruction itself.

Example: STA 6500H;

3) Indirect Addressing Mode:

In indirect addressing mode the address(16-bit) of operand(data) is specified by a register pair. The address stored in register pair points to memory location.

Example: 1) LXI H, 7500H; 2) MOV A,M

4) Immediate Addressing Mode:

In immediate addressing mode the data (8-bit/16bit) or operand is specified within the instruction itself or it is aa part of instruction.

Example: 1) MVI A, 35H; 2) LXI D, 3211H;

5) Implicit or Implied Addressing Mode:

In implied or implicit addressing mode the operand is not specified in the instruction i.e. operand is absent in instruction. The operand is specified within the opcode itself. The data(operand) is supposed to be present generally in accumulator.

Example: 1) RAL ; 2) RLC ; 3) CMA ;

Classification of Instruction of 8085 microprocessor

Q8) How instructions of 8085 microprocessor are classified?

The 8085 instructions are classified according to its operations as like six different groups such as follows:

i) Data Transfer Group

The instructions of this group transfers data from source to destination without altering the contents of source. The contents of flags are not affected by any instruction in this group.

ii) Arithmetic Group

The instructions of this group perform arithmetic operation such as addition, subtraction, increment, decrement etc of the content of register or memory. Almost all the instructions in this group affect the zero, sign, parity, carry and auxillary carry flag according to the flag definattion.

All subtraction operations are performed using 2's compilement and set if borrow or not.

iii) Logical Group

The instructions of this group perform logical operation such as AND, OR, Ex-OR, Compare, rotate, compliment etc of data in register or memory.

iv) Branch Control Group

The instructions of this group change the normal sequence of the program. These are two types of branch instructions:

a) Unconditional Branch Instruction:

The unconditional branch instructions transfer the program to the specified label or address unconditionally i.e. without satisfying any condition.

b) Conditional Branch Instruction:

The conditional branch instruction transfer the program to the specified label or address when certain condition is satisfied. The condition is tested depending upon the status of zero, parity, sign and carry flags. The program counter contains the address of next instruction to be executed. The branch control group instruction loads the new address in PC to execute the program from new address.

v) Stack, I/O and Machine control Group:

The instruction of this group perform I/O data transfer, manipulates the stack and perform machine related operations.

vi) Interrupt Control Group:

The instructions of this group performs interrupt related operations.

Data Transfer Group

The instructions of this group transfers data from source to destination without altering the contents of source. The contents of flags are not affected by any instruction in this group.

1) MOV r1,r2

Function:	**[r1] ← [r2]** The content of register r2 is moved or copies to register r1.
Length	1 byte
Addressing mode	Register
Flags affected	No flags are affected.
Example	MOV A, B

2) MOV r,M

Function:	**[r] ← [HL]** The content of memory whose address is in register pair HL is moved or copies to register r.
Length	1 byte
Addressing mode	Indirect
Flags affected	No flags are affected.
Example	MOV B, M

3) MOV M,r

Function:	**[HL] ← [r]** The content of register r is moved or copies to the memory whose address is in register pair.
Length	1 byte
Addressing mode	Indirect
Flags affected	No flags are affected.
Example	MOV M, B

4) MVI r,data

Function:	**[r] ← [8bit data]** The 8bit data is given in instruction is copy or moves to register given in instruction.
Length	**2** byte
Addressing mode	Immediate
Flags affected	No flags are affected.
Example	MVI E, 14H

5) MVI M,data

Function:	**[HL] ← [8bit data]** The 8bit data is given in instruction is copy or moves to the memory location whose address is in HL register pair.
Length	**2** byte
Addressing mode	Immediate
Flags affected	No flags are affected.
Example	MVI M, 25H

6) LXI rp,16bit data

Function:	**[rp] ← [16bit data]** **[rh]← 8MSBs of data** **[rl]← 8LSBs of data** The 16bit data is given in instruction is copy or moves to register pair given in instruction.
Length	**3** byte
Addressing mode	Immediate
Flags affected	No flags are affected.
Example	LXI H, 2300H

7) LDA addr

Function:	**[A] ← [addr]** The content of memory location is given in instruction is copy or move or loaded into accumulator i.e. A register.
Length	**3** byte
Addressing mode	Direct
Flags affected	No flags are affected.
Example	LDA 2300H

8) STA addr

Function:	**[addr] ← [A]** The content of accumulator is stored in the memory location whose address is specified in instruction.
Length	**3** byte
Addressing mode	Direct
Flags affected	No flags are affected.
Example	STA C500H

9) LHLD addr

Function: **[L] ← [addr]**
[H] ← [addr+1]
The content of memory location whose address is specified in the instruction is loaded or copy or moves into register L as well as content of next memory location i.e. address is given instruction+1 is loaded into register H.

Length **3** byte
Addressing mode Direct
Flags affected No flags are affected.
Example LHLD 2900H

10) SHLD addr

Function: **[addr] ← [L]**
[addr+1]← [H]
The content of L is stored in the memory location whose address is specified in the instruction. The content of register H is stored in the next memory location i.e. addr+1.

Length **3** byte
Addressing mode Direct
Flags affected No flags are affected.
Example SHLD 3900H

11) LDAX rp

Function: **[A] ← [rp]**
The content of memory location whose address is in the register pair rp is loaded or moves or copies into the accumulator.

Length **1** byte
Addressing mode Indirect
Flags affected No flags are affected.
Example LDAX B

12) STAX rp

Function: **[rp] ← [A]**
The content of accumulator is stored or moves or copies in the memory location whose address is in the register pair rp.

Length **1** byte
Addressing mode Indirect
Flags affected No flags are affected.
Example STAX D

13) XCHG

Function: **[HL] ←> [DE]**
Length 1 byte
Addressing mode Register
Flags affected No flags are affected.
Example XCHG

Arithmetic Group

The instructions of this group perform arithmetic operation such as addition, subtraction, increment, decrement etc of the content of register or memory. Almost all the instructions in this group affect the zero, sign, parity, carry and auxillary carry flag according to the flag definattion.

All subtraction operations are performed using 2's compilement and set if borrow or not.

14) ADD r

Function: **[A] ← [A]+[r]**
Whenever this type of an instruction is executed then content of register given in instruction added with content of A register and result(sum) is stored in accumulator i.e. A register.

Length: 1byte
Addressing mode: Register
Flags affected: All flags are affected.
Example: ADD B

15) ADD M

Function: [A]← [A]+[HL]
Whenever this type of an instruction is executed then content of HL is added with content of register A and result(sum) is stored in accumulator i.e. A register.
Length: 1 byte
Addressing mode: Indirect
Flags affected: All flags are affected.
Example: ADD M

16) ADI data

Function: **[A]← [A]+[8-bit data]**
Whenever this type of an instruction is executed then 8-bit data given in instruction is added to content of register A and result(sum) is stored in accumulator i.e. A register.
Length: 2 byte
Addressing mode: Immediate
Flags affected: All flags are affected.
Example: ADI 24H

17) ADC r

Function: **[A]←[A]+[r]+[cy]**
Whenever this type of an instruction is executed then content of carry and content of register given in instruction is added to register A and result(sum) is stored into accumulator i.e. A register.
Length: 1 byte
Addressing mode: Register
Flags affected: All flags are affected.
Example: ADC B

18) ADC M

Function: **[A]←[A]+[HL]+[cy]**
Whenever this type of an instruction is executed then content of HL and carry content are added to register A content and result (sum) is stored into A register i.e. accumulator.
Length: 1 byte
Addressing mode: Indirect
Flags affected: All flags are affected.
Example: ADC M

19) ACI data

Function: **[A]←[A]+[8-bit data]+[cy]**
Whenever this type of an instruction is executed then 8-bit data given in instruction and content of carry is added to content of register A i.e. accumulator and result(sum) is stored into register A i.e. accumulator.
Length: 2 byte
Addressing mode: Immediate
Flags affected: All flags are affected.
Example: ACI 26H

20) DAD rp

Function: **[HL]←[HL]+[rp]**
Whenever this type of an instruction is executed then content of register pair i.e. rp are added to the content of HL register pair.
Length: 1 byte
Addressing mode: Register
Flags affected: Only carry
Example: DAD B

21) SUB r

Function: **[A]←[A]–[r]**

Whenever this type of an instruction is executed then content of register given in instruction is subtracted from the content of an accumulator i.e. A register. The result(diff) is stored in an accumulator i.e. register A.

Length: 1 byte
Addressing mode: Register
Flags affected: All flags are affected.
Example: SUB C

22) SUB M

Function: **[A]←[A]–[HL]**

Whenever this type of an instruction is executed then content of HL register pair given in instruction is subtracted from the content of an accumulator i.e. A register. The result(diff) is stored in an accumulator i.e. register A.

Length: 1 byte
Addressing mode: Indirect
Flags affected: All flags are affected.
Example: SUB M

23) SUI data

Function:

Whenever this type of an instruction is executed then 8-bit data is given in instruction is subtracted from the content of an accumulator i.e. A register. The result(diff) is stored in an accumulator i.e. register A.

Length: 2byte
Addressing mode: Immediate
Flags affected: All flags are affected.
Example: SUI 21H

24) SBB r

Function:

Whenever this type of an instruction is executed then content of register given in instruction and content of borrow is subtracted from the content of an accumulator i.e. A register. The result(diff) is stored in an accumulator i.e. register A.

Length: 1 byte
Addressing mode: Register
Flags affected: All flags are affected.
Example: SBB E

25) SBB M

Function:

Whenever this type of an instruction is executed then content of HL register pair given in instruction and content of borrow is subtracted from the content of an accumulator i.e. A register. The result(diff) is stored in an accumulator i.e. register A.

Length: 1 byte
Addressing mode: Indirect
Flags affected: All flags are affected.
Example: SBB M

26) SBI data

Function:

Whenever this type of an instruction is executed then content of 8-bit data is given in instruction and content of borrow is subtracted from the content of an accumulator i.e. A register. The result(diff) is stored in an accumulator i.e. register A.

Length: 2 byte
Addressing mode: Immediate
Flags affected: All flags are affected.
Example: SBI 2EH

27) INR r

Function: **[r]←[r]+1**
Whenever this type of an instruction is executed then content of register 'r' is incremented by one and incremented result stores into same register.

Length: 1 byte
Addressing mode: Register
Flags affected: Except carry flag all other flags other are affected.
Example: INR B

28) INR M

Function: **[HL]←[HL]+1**
Whenever this type of an instruction is executed then content of memory location addressed by HL pair is incremented by one and incremented result is stored into same HL memory location.

Length: 1 byte
Addressing mode: Indirect
Flags affected: Except carry flag all other flags are affected.
Example: INR M

29) INX rp

Function: **[rp]←[rp]+1**
Whenever this type of an instruction is executed then content of register pair rp is incremented by one and incremented result is stored into same register pair.

Length: 1 byte
Addressing mode: Register
Flags affected: No flags are affected.
Example: INX H

30) DCR r

Function: **[r]←[r]-1**
Whenever this type of an instruction is executed then content of register 'r' is decremented by one and decremented result stores into same register.

Length: 1 byte
Addressing mode: Register
Flags affected: Except carry flag all other flags are affected.
Example: DCR B

31) DCR M

Function: **[HL]←[HL] – 1**
Whenever this type of an instruction is executed then content of memory location addressed by HL pair is decremented by one and decremented result is stored into same HL memory location.

Length: 1 byte
Addressing mode: Indirect
Flags affected: Except carry flag all other flags are affected.
Example: DCR M

32) DCX rp

Function: **[rp]←[rp] – 1**
Whenever this type of an instruction is executed then content of register pair rp is decremented by one and decremented result is stored into same register pair.

Length: 1 byte
Addressing mode: Register
Flags affected: No flags are affected.
Example: DCX B

33) DAA

Function: The DAA instruction convert the binary(Hex) result in an accumulator into decimal or BCD result. The instruction DAA is used in the program after ADD, ADI, ACI, ADC instructions only. The followings steps are taken to convert binary result to decimal result.
Step 1: If the value of 4 LSBs (Lower nibble) of greater than 9 OR AC flag is set to 1 then DAA adds 06H in content of Accumulator.
Step 2: If the value of 4 MSBs (Higher nibble) of greater than 9 OR CY flag is set to 1 then DAA adds 60H in content of Accumulator.

Length: 1 byte
Addressing mode: Implicit or Implied
Flags affected: All flags are affected.
Example: DAA

Logical Group

The instructions of this group perform logical operation such as AND, OR, Ex-OR, Compare, rotate, compliment etc of data in register or memory.

34) ANA r

Function: **[A] ← [A] ^ [r]**
Whenever this type of an instruction is executed then content of register 'r' is logically ANDed with the content of an accumulator i.e. A register. The result(ANDing content) is always stored into accumulator or A register.

Length: 1 byte
Addressing Mode: Register
Flags affected: All flags are affected. After ANDing Some flags are modified again such as CY=0 and AC=1
Example: ANA E

35) ANA M

Function: **[A] ← [A] ^ [HL]**
Whenever this type of an instruction is executed then content of memory location is addressed by HL pair is logically ANDed with the content of an accumulator i.e. A register. The result(ANDing content) is always stored into accumulator or A register.

Length: 1 byte
Addressing Mode: Indirect
Flags affected: All flags are affected. After ANDing Some flags are modified again such as CY=0 and AC=1
Example: ANA M

36) ANI data

Function: **[A] ← [A] ^ [8-bit data]**
Whenever this type of an instruction is executed then 8-bit data is given in instruction is logically ANDed with the content of an accumulator i.e. A register. The result(ANDing content) is always stored into accumulator or A register.

Length: 2 byte
Addressing Mode: Immediate
Flags affected: All flags are affected. After ANDing Some flags are modified again such as CY=0 and AC=1
Example: ANI 2BH

37)ORA r

Function:	**[A] ← [A] V [r]** Whenever this type of an instruction is executed then content of register 'r' is logically ORed with the content of an accumulator i.e. A register. The result(ORing content) is always stored into accumulator or A register.
Length:	1 byte
Addressing Mode:	Register
Flags affected:	All flags are affected. After ORing Some flags are modified again such as CY=0 and AC=0
Example:	ORA D

38) ORA M

Function:	**[A] ← [A] V [HL]** Whenever this type of an instruction is executed then content of memory location is addressed by HL pair is logically ORed with the content of an accumulator i.e. A register. The result(ORing content) is always stored into accumulator or A register.
Length:	1 byte
Addressing Mode:	Indirect
Flags affected:	All flags are affected. After ORing Some flags are modified again such as CY=0 and AC=0
Example:	ORA M

39) ORI data

Function:	**[A] ← [A] V [8-bit data]** Whenever this type of an instruction is executed then 8-bit data is given in instruction is logically ORed with the content of an accumulator i.e. A register. The result(ORing content) is always stored into accumulator or A register.
Length:	2 byte
Addressing Mode:	Immediate
Flags affected:	All flags are affected. After ORing Some flags are modified again such as CY=0 and AC=0
Example:	ORI 2CH

40) XRA r

Function:	**[A] ← [A] ∀ [r]** Whenever this type of an instruction is executed then content of register 'r' is logically XORed with the content of an accumulator i.e. A register. The result(XORing content) is always stored into accumulator or A register.
Length:	1 byte
Addressing Mode:	Register
Flags affected:	All flags are affected. After XORing Some flags are modified again such as CY=0 and AC=0
Example:	XRA E

41) XRA M

Function: **[A] ← [A] ∀ [HL]**
Whenever this type of an instruction is executed then content of memory location is addressed by HL pair is logically XORed with the content of an accumulator i.e. A register. The result(XORing content) is always stored into accumulator or A register.

Length: 1 byte
Addressing Mode: Indirect
Flags affected: All flags are affected. After XORing Some flags are modified again such as CY=0 and AC=0
Example: XRA M

42) XRI data

Function: **[A] ← [A] ∀ [8-bit data]**
Whenever this type of an instruction is executed then 8-bit data is given in instruction is logically XORed with the content of an accumulator i.e. A register. The result(XORing content) is always stored into accumulator or A register.

Length: 2 byte
Addressing Mode: Immediate
Flags affected: All flags are affected. After XORing Some flags are modified again such as CY=0 and AC=0
Example: XRI 2DH

43) CMA Compliment accumulator

Function: $A \leftarrow [\overline{A}]$
Whenever this type of an instruction is executed then content of an accumulator is complimented i.e. 1's compliment result is obtained. The complimented (1'scomplimnet) is stored into accumulator.

Length: 1 byte
Addressing Mode: Implicit or Implied
Flags affected: No flags are affected.
Example: CMA

44) CMC

Function: $CY \leftarrow [\overline{CY}]$
Whenever this type of an instruction is executed then content of only carry flag is complimented and carry compliment is stored into same carry flag.

Length: 1 byte
Addressing Mode: Implicit or Implied
Flags affected: Only carry
Example: CMC

45) STC

Function: **[CY] ← 1**
Length: 1 byte
Addressing Mode: Implicit or Implied
Flags affected: Only Carry
Example: STC

46) CMP r

Function: **[A] – [r]**
Whenever this type of instruction is executed then content of register 'r' is subtracted from the content of an accumulator. The result is not stored anywhere. The content of flags will affected according to the result of subtraction such like as follows:
i) if A > r then CY=0
ii) if A< r then CY=1
iii) if A= r then Z=1

Length: 1 byte
Addressing Mode: Register
Flags affected: All flags are affected.
Example: CMP B

47) CMP M

Function: **[A] – [HL]**
Whenever this type of instruction is executed then content of memory location is addressed by HL pair is subtracted from the content of an accumulator. The result is not stored anywhere. The content of flags will affected according to the result of subtraction such like as follows:
i) if A > HL then CY=0
ii) if A< HL then CY=1
iii) if A= HL then Z=1

Length: 1 byte
Addressing Mode: Indirect
Flags affected: All flags are affected.
Example: CMP M

48) CPI data

Function: **[A] – [8-bit data]**
Whenever this type of instruction is executed then 8-bit data is given in instruction is subtracted from the content of an accumulator. The result is not stored anywhere. The content of flags will affected according to the result of subtraction such like as follows:
i) if A > 8-bit data then CY=0
ii) if A< 8-bit data then CY=1
iii) if A= 8-bit data then Z=1

Length: **2** byte
Addressing Mode: Immediate
Flags affected: All flags are affected.
Example: CPI 26H

49) RLC **Rotate accumulator left**

Function: $[D_{n+1}] \leftarrow [D_n]$
$[D_0] \leftarrow [D_7]$
$[CY] \leftarrow [D_7]$
Whenever this type of an instruction is executed then content of accumulator is rotated towards left by one bit. The seventh bit of accumulator is moved to carry bit as well as to the zero bit of the accumulator as shown if following figure

Length: 1 byte
Addressing Mode: Implicit or Implied
Flags affected: Only Carry is affected.
Example: RLC

50) RAL

Function: $[D_{n+1}] \leftarrow [D_n]$
$[CY] \leftarrow [D_7]$
$[D_0] \leftarrow [CY]$
Whenever this type of an instruction is executed then content of accumulator is rotated towards left through carry by one bit. The seventh bit of accumulator is moved to carry and carry bit is moved to zero bit of accumulator as shown if following figure

Length: 1 byte
Addressing Mode: Implicit or Implied
Flags affected: Only Carry flag is affected.
Example: RAL

51) RRC

Function: **$[D_{n-1}] \leftarrow [D_n]$**
$[D_7] \leftarrow [D_0]$
$[CY] \leftarrow [D_0]$
Whenever this type of an instruction is executed then content of accumulator is rotated towards right by one bit. The zero bit of accumulator is moved to seventh bit the accumulator as well as to carry bit as shown if following figure

Length: 1 byte
Addressing Mode: Implicit or Implied
Flags affected: Only Carry is affected.
Example: RRC

52) RAR

Function: **$[D_{n-1}] \leftarrow [D_n]$**
$[CY] \leftarrow [D_0]$
$[D_7] \leftarrow [CY]$
Whenever this type of an instruction is executed then content of accumulator is rotated towards right by one bit through carry. The zero bit of accumulator is moved to carry and the carry bit is moved to seventh bit of accumulator as shown if following figure

Length: 1 byte
Addressing Mode: Implicit or Implied
Flags affected: Only Carry is affected.
Example: RAR

Branch Control Group:

The instructions of this group change the normal sequence of the program. There are two types of branch instruction.

1) **Unconditional Branch Instructions:**
   The unconditional branch instructions transfers the program to the specified label or address unconditionally i.e. without satisfying any condition.
2) **Conditional Branch Instructions:**
   The conditional branch instructions transfer the program to the specified label or address when certain condition is satisfied.
   The condition is tested depending upon the status of zero(Z), Parity(P), Sign(S), and Carry (CY) flags. The program counter (PC) contains the address of next instructions to be executed. The branch control group instruction loads the new address in PC to execute the program from new address.

Unconditional Branch Control Instruction:

54) JMP addr (label) Unconditional Jump

Function: **[PC] ← addr**
Whenever this type of instruction then it jump to the address of the label unconditionally. The address of the label is the address of memory location for next instruction to be executed. This instruction load the address of label in program counter.

Length: 3 byte
Addressing mode: Immediate
Flags affected: No flags are affected.
Example: JMP C523H

Conditional Branch Control Instruction:

In conditional jump instructions if the condition is true or satisfied then only jump is made at the specified address. If condition is false or not satisfied then the next instruction in the sequence is executed. The conditional jump instruction are given below:

Jcondition addr/label

Function

if condition is true then

PC ← addr (label)

else

PC← PC+3

i.e. it executes next instruction in sequence.

Length : 3 byte.

Addressing mode: Immediate

Flags affected : No flags are affected.

Instructions conditional jumps:

55) JZ addr (LABEL)

Jump if the result is zero i.e. Z=1.

56) JNZ addr (LABEL)

Jump if the result is not zero i.e. Z=0.

57) JC addr (LABEL)

Jump if the result is carry i.e. CY=1.

58) JNC addr (LABEL)

Jump if the result is no carry i.e. CY=0.

59) JP addr (LABEL)

Jump if the result is plus i.e. S=0.

60) JM addr (LABEL)

Jump if the result is minus i.e. S=1.

61) JPE addr (LABEL)

Jump if even parity i.e. P=1.

62) JPO addr (LABEL)

Jump if odd parity i.e. P=0.

Unconditional Call Instruction

63) CALL addr/Label (Unconditional Call)

Format: **[SP-1] ← [PCH]**
[SP-2]← [PCL]
[SP]←[SP-2]
[PC]←addr / label

Whenever this type of instruction is executed then it call subroutine or subprogram. Before calling to the subroutine the address of next instruction of the main program is saved in the stack. The content of the stack pointer is decremented by two. Then the program jumps to subroutine or subprogram starting at address specified by label.

Thus program counter stores address given in instruction.

Length: 3 byte.

Addressing Mode: Immediate / Indirect

Flags affected: No flags are affected.

Example CALL C050H

Conditional CALL instructions:

In conditional CALL instruction if condition is true then program calls the specified subroutine or subprogram. If the condition is false then the next instruction in the sequence is executed. Before call the address if next instruction of the main program is saved in the stack. The stack pointer is decremented by two memory location.

Thus program counter stores address given in instruction if given condition is true. If false then next instruction in program is executed i.e. PC contains address of next instruction in main program.

Ccondition addr / label

Function: If condition is true then
[SP-1]← PCH
[SP-2]← PCL
[SP]← SP – 2
[PC]← addr / label
else
PC←PC+3
i.e. executes the next instruction in the main program.

Length: 3 byte.
Addressing mode: Immediate / Indirect
Flags affected No flags are affected.

The conditional CALL instructions are as given below:

64) CZ addr (LABEL)
Calls a subroutine if the result is zeo i.e. Z=1.

65) CNZ addr (LABEL)
Calls a subroutine if the result is not zeo i.e. Z=0.

66) CC addr (LABEL)
Calls a subroutine if the result is contains carry i.e. CY=1.

67) CNC addr (LABEL)
Calls a subroutine if the result is not contain carry i.e. CY=0.

68) CP addr (LABEL)
Calls a subroutine if the result is Plus i.e. S=0.

69) CM addr (LABEL)
Calls a subroutine if the result is negative or minus i.e. S=1.

70) CPE addr (LABEL)
Calls a subroutine if the result is even parity i.e. P=1.

71) CPO addr (LABEL)
Calls a subroutine if the result is Odd parity i.e. P=0.

Unconditional Return Instruction:

72) RET Unconditional Return
RET

Format : **[PCL] ← [SP]**
[PCH]← [SP+1]
[SP]← [SP+2]
Whenever this type of instruction is executed then it return from subroutine. The RET instruction is used at the end of subroutine. Before the execution of a subroutine the address of the next instruction of the main program is saved in the stack. The execution of RET instruction brings back the saved address from the stack to the program counter. The content of stack pointer is incremented by 2. Then the program jumps to the next instruction after CALL in the main program.

Length : 1 byte
Addressing Mode : Indirect
Flags affected : No flags are affected.
Example: RET

Conditional RET instruction:

In conditional RET instruction if condition is true then the program returns form the subroutine. If condition is false then the next instruction in the sequence is executed.

Rcondition

Function: **i**f condition is TRUE then
[PCL] ← [SP]
[PCH]← [SP+1]
[SP]← SP+2
else
PC←PC+1
i.e. executes the next instruction in the sequence.

Length: 1 byte.
Addressing Mode: Indirect.
Flags affected: No flags are affected.
Example: **RC**

The conditional RET instructions are as given below:

73) RZ Return from subroutine if the result is zero i.e. Z=1.

74) RNZ Return from subroutine if the result is not zero i.e. Z=1.

75) RC Return from subroutine if the result is contains carry i.e. CY=1.

76) RNC Return from subroutine if the result is not contains carry i.e. CY=0.

77) RP Return from subroutine if the result is plus i.e. S=0.

78) RM Return from subroutine if the result is minus or negative i.e. S=1.

79) RPE Return from subroutine if the result is even parity i.e. P=1.

80) RPO Return from subroutine if the result is odd parity i.e. P=0.

Stack Group Instructions:

81) PUSH rp

Function : **[SP-1] ← [rh]**
[SP-2] ← [rl]
SP ← SP – 2

Whenever this type of an instruction is executed then the content of register pair rp is pushed or copied onto the stack. The stack pointer is decremented by one and the contents of higher order of rp are copied into that location. The stack pointer is again decremented by 1 i.e. SP-2 and the contents of lower order register of rp are copied at that location. The rp can be like BC/DE/HL.

Length: 1 byte.
Addressing Mode: Indirect.
Flags affected: No flags are affected.
Example: PUSH B

82) PUSH PSW

Function : **[SP-1]← [A]**
[SP-2] ← [flags or PSW]
[SP] ← [SP – 2]

Whenever this type of instruction is executed then content of processor status word or program status word (PSW) is pushed or copied onto the stack. The stack pointer is decremented by one and the contents of accumulator are copied onto that location. The stack pointer is again decremented by one i.e. SP-2 and the content of flags or program status word(PSW) are copied at that location.

Length : 1 byte.
Addressing Mode : Indirect
Flags affected : No flags are affected.
Example: PUSH PSW

83) POP rp

Function : ` **[rl] ← [SP]**
[rh] ← [SP+1]
[SP] ← SP+2

Whenever this type of instruction is executed then POP the content of register pair i.e. rp from the stack. The contents of memory location pointed by SP are copied to the lower order register of rp. The SP is incremented by one and content of that memory location are copied to the higher order register of rp. The SP is again incremented by one i.e SP+2. The rp can be one of BC/HL/DE.

Length : 1 byte.
Addressing Mode : Indirect.
Flags affected: No flags are affected.
Example: POP B

84) POP PSW

Function: **[flags or PSW] ← [SP]**
[A] ← [SP+1]
[SP] ← SP+2

Whenever this type of instruction is executed then POP the content of processor status word or program status word (PSW) from the stack. The contents of memory location pointed by SP are copied to the flags or program status word (PSW). The SP is incremented by one and content of that location is stored or copied.to the accumulator. The SP is again incremented by one i.e. SP+2.

The POP process is exactly opposite to PUSH. So the contents are stored by PUSH are taken back using POP instructions.

Length: 1 byte.
Addressing Mode: Indirect.
Flags affected: No flags are affected.
Example: POP PSW

85) XTHL

Function: **[L] <-> [SP]**
[H] <-> [SP + 1]

Whenever this type of instruction is executed then it exchanges stack top with HL pair. The contents of L register are exchanged with stack location pointed by stack pointer. The content of H register are exchanged with the next stack location. The contents of the stack pointer register are not altered or affected.

Length: 1 byte.
Addressing Mode: Indirect.
Flags affected: No flags are affected.
Example: XTHL

86) SPHL

Function: **[SP]← [HL]**

Whenever this type of instruction is executed then the content of HL register pair are moved to the SP register.

Length: 1 byte.
Addressing Mode: Register.
Flags affected: No flags are affected.
Example: SPHL

Input/Output Group Instructions:

87) IN port addr

Function: **[A] ← [port address]**

Whenever this type of instruction is executed then content of port given in instruction is moved or copied to the accumulator. After the instruction IN the address of port is specified. The address of a port is an 8-bit input port address.

Length: 2 byte.
Addressing Mode: Direct.
Flags affected: No flags are affected.
Example: IN 10H

88) OUT port addr

Function: **[port] ← [A]**

Whenever this type of instruction is executed then content of accumulator is moved or copied to the port i.e output port. After the instruction OUT the address of port is specified. The address of a port is an 8-bit address.

Length: 2 byte.
Addressing mode: Direct.
Flags affected: No flags are affected.
Example: OUT 10H

Machine Control Instructions

89) HLT Halt
Function: **HALT**
Whenever this type instruction is executed then it stops the microprocessor. The registers and status flags remains unaffected.
Length: 1 byte.
Addressing Mode: None
Flags affected: No flags are affected.
Example: HLT

90) NOP **No operation**
Function: Whenever this type of instruction is executed then no operation is performed. The registers and flags remains unaffected.
Length: 1 byte.
Addressing Mode: None
Flags affected: No flags are affected.
Example: NOP

Interrupt Control Group:

91) RST n **Restart (n is from 0 to 7)**
Function **[SP–1] - ← PCH**
[SP–2] ← PCL
[SP] ← SP–2
[PC] ← 8 times n
Whenever this type of an instruction is executed then it transfers the program control to specific memory location known as restart location or restart address. Restart is a one word CALL instruction. The restart address are referred as vectored addresses. The microprocessor multiplies the RST by 8 to estimate these vector address as shown in following table.
Before transferring the program control to the vector address the contents of program counter is saved on the stack like CALL instruction. This instruction can be used as software interrupt.

Length: 1 byte.
Addressing Mode Indirect
Flags affected No flags are affected.

Instructions OR Software Interrupt Instructions	**Restart Address OR Vector Address Or Software Interrupt Address**
RST 0	0000H
RST 1	0008H
RST 2	0010H
RST 3	0018H
RST 4	0020H
RST 5	0028H
RST 6	0030H
RST 7	0038H

Example : RST 1

92) EI **Enable Interrupt**
Function: Whenever this type instruction is executed then the interrupt system is enabled.
Length: 1 byte.
Addressing mode No addressing mode.
Flags affected: No flags are affected.
Example **EI**

93) DI **Disable Interrupt**
Function: Whenever this type instruction is executed then the interrupt system is disabled.
Length: 1 byte.
Addressing mode No addressing mode.
Flags affected: No flags are affected.
Example **DI**

94) SIM **Set Interrupt Mask.**

Function: The execution of the SIM enables/disables interrupts according to the bit pattern of the accumulator. This instruction is also used for serial data communication on SOD pin of 8085. The following is accumulator contents for SIM instructions OR interprt's meaning of

D7	D6	D5	D4	D3	D2	D1	D0
SID	I 7.5	I 6.5	I 5.5	IE	M 7.5	M 6.5	M 5.5

SIM

1) SOD : Serial Data Output
2) SDE: Serial Data Enable
if 1 then serial data is enabled.
if 0 then serial data is disabled.
3) R7.5 : Reset RST 7.5.
if 1 then RST 7.5 is reset.
if 0 then RST 7.5 is ser.
4) MSE : Mask set enable.
if 1 then mask set enable is enabled.
if 0 then mask set enable is disabled.
5) M7.5 : RST 7.5 Mask.
if 1 then RST 7.5 is masked or made for pending or disabled.
if 0 then RST 7.5 is non masked or not made for pending or enabled.
6) M6.5 : RST 6.5 Mask.
if 1 then RST 6.5 is masked or made for pending or disabled.
if 0 then RST 6.5 is non masked or not made for pending or enabled.
7) M 5.5 : RST 5.5 Mask.
if 1 then RST 5.5 is masked or made for pending or disabled.
if 0 then RST 5.5 is non masked or not made for pending or enabled.

Length 1 byte.
Addressing mode: No addressing mode.
Flags affected: No flags are affected.
Example **SIM**

95) RIM **Read Interrupt Mask.**

Function: Whenever this instruction is executed then the content of an accumulator is loaded with status of pending interrupt. The status of restart interrupt mask and the contents of SID (serial input data). The following fig shows the accumulator contents for RIM instruction:

D7	D6	D5	D4	D3	D2	D1	D0
SOD	SDE	X	R7.5	MSE	M7.5	M6.5	M5.5

1) SID : Serial Input Data.
2) I 7.5 : Pending RST 7.5.
if 1 then RST 7.5 is made for pending or disabled.
if 0 then RST 7.5 is not made for pending or enabled.
3) I 6.5 : Pending RST 6.5.
if 1 then RST 6.5 is made for pending or disabled.
if 0 then RST 6.5 is not made for pending or enabled.
4) I 5.5 : Pending RST 5.5.
if 1 then RST 5.5 is made for pending or disabled.
if 0 then RST 5.5 is not made for pending or enabled.
5) IE : Interrupt Enable Flag.
if 1 then interrupt enable flag is enabled.
if 0 then interrupt enable flag is disabled.
6) M 7.5 : RST 7.5 Mask.
if 1 then RST 7.5 is masked or made for pending or disabled.
if 0 then RST 7.5 is non masked or not made for pending or enabled.
7) M 6.5 : RST 6.5 Mask.
if 1 then RST 6.5 is masked or made for pending or disabled.
if 0 then RST 6.5 is non masked or not made for pending or enabled.
8) M 5.5 : RST 5.5 Mask.
if 1 then RST 5.5 is masked or made for pending or disabled.
if 0 then RST 5.5 is non masked or not made for pending or enabled.

Length: 1 byte.
Addressing mode No addressing mode.
Flags affected: No flags are affected.
EXAMPLE RIM

Q1) The flag register of 8085 microprocessor (µP) contains data 45H. Then interpret's its meaning(M2002)

Q2) In 8085 microprocessor (µP) the flag register content is 3CH. Then Interpret's its meaning(M2004)

Q3) The flag register of 8085 microprocessor (µP) contains data B5H. Then Interpret's its meaning(M2005)

Q4) Explain any three flags available in 8085 microprocessor (µP). If the flag register contains CAH. Interpret's its meaning(O2008)

Q5) In flag register contents are C1H and 84H then interpret's its meaning separately.(O2006)

Q1) The accumulator in 8085 contains data B8H & register B contains data 40H. What will be the contents of Accumulator after execution of each of the following instructions independently (M2002)
a) RLC b)ORI 29H c) ANA B

Q2) The accumulator contains data AAH & register D contains data 55H.What will be the contents of an accumulator in hex after execution of each of the following instructions independently
a) ANA D b)XRA D c) ADI 81H
d) ORA D (M2003)

Q3) The accumulator contains data 43H. What will be it's contents after execution of the following instructions independently?
a) CMA b) ANI 09H c) INR A

Q4) The accumulator of 8085 contains data 45H & register E contains data 7BH. What will be the contents of an accumulator, after execution of each following instructions independently:
a) XRA E b) ADI C5H c) ORI 5BH (Mar 2004)

Q5) Acc of 8085 contains data 56H. What will be the contents after execution of each of following instruction independently?
a) CMA b) ANI ACH c) INR A
(Mar 2005)

Q6) If accumulator contains data BCH, register C contains data ADH. What will be the content of ACC after execution of the following instruction independently:
a) SUB C b) CMA c)XRA C (M-2006)

Q7) If acc contains the data BBH & register D contains data 99H. What will be the contents of an accumulator after execution of each of following instruction independently:
a) ORA D b) RRC c) ADD D (0ct-2006)

Q8) The accumulator of 8085 contains data ABH & register B contains BAH. What will be the contents of an accumulator after execution of each of the following instruction independently:
a) ORA B b) XRA B c) ANI OFH (Oct-2007)

Q9) The accumulator contains data ABH. What will be the contents after execution of following instruction independently:
a) XRI B5H b) CMA c) SUB A (M2008)

Q10) Acc contains data E4H. What will be the contents of an accumulator after stepwise execution of each of the following instruction : (Oct 2008)
a) ANI 58H b) RRC c) CMA

Q11) The Acc of 8085 contains data E5H & register B contains 3EH. What will be the content of the ACC after execution of each of the following instruction independently :
a) ANA B b) XRA B c) SUB B (M-2009)

Q12) Acc contains 45H, register E contains data 3BH. Write the contents of an Acc after execution of following instruction independently : (Oct-2009)
a) SUB E b) XRA E c) RRC
d) MOV E, A

Q13) The ACC contains 05H & register B contains 08H. What will be the effect of SUB B instruction on flags? Explain it with diagram? (M-2010)

Notifications and their Meaning used in 8085 microprocessor in instruction set

F	It means flag register which is 8 bit .
A	It means A register or Accumulator/ACC which is 8 bit .
B	It means B register which is 8 bit .
C	It means C register which is 8 bit .
D	It means D register which is 8 bit .
E	It means E register which is 8 bit .
H	It means H register which is 8 bit .
L	It means L register which is 8 bit .
SP	Stack pointer which 16-bit. In 8085 it is available in two order such as SPH is 8-bit high order and SPL 8-bit low order.
PC	Program Counter which 16-bit pointer register. In 8085 it is available in two order such as PCH is 8-bit high order and PCL 8-bit low order.
r1,r2	These are destination register and source register respectively. The destination and source is separated by comma(,). So r1 is destination register where as r2 is source register both are specified as one of register such A or B or C or D or E or H or L.
M	It means memory register, which addressed by HL pair i.e. The content of M is stored to HL location.
data	It is 8-bit immediate data it may be one of from 00H to FF data series. It is specified only in source location not destination location.
Rp	It is register pair which is combination of two register & capable to store 16-bit data. In 8085 the valid register pairs are such as follows: a) BC rp : in which B is a 8-bit high order register in register pair and C is a also 8-bit low order register in register pair. b) DE rp in which D is a 8-bit high order register in register pair and E is a also 8-bit low order register in register pair. c) HL rp in which H is a 8-bit high order register in register pair and L is a also 8-bit low order register in register pair. Sometimes in special situation SP rp is also used which is not valid register pair
addr	It is a address or memory location which is any 16-bit immediate data or 16-bit memory location may be from 0000H to FFFFH location
^	It is a ANDing symbol, which performs ANDing operation
V	It is a ORing symbol, which performs ORing operation
∀	It is a XORing symbol, which performs XORing operation

1)A block of data is stored from M.L. 2001H & onwards. The count is stored at M.L. 2000H. Write an ALP to find out sum of the data items stored in a block. Stores the result at M.L. 2500H & onwards starting with LSB. (Mar-2002)

2) Write an ALP to add two BCD numbers stored at M.L. 3500H and 3501H. Place the BCD result in M.L. 3502H & onwards starting with L.S.B.(Mar-2002)

3) Write an ALP to subtract the number stored in M.L. 3601H from number stored in M.L. 3600H. Stores the +ve result at M.L. 3602H.(Mar 2002)

4) Write an ALP to count number of even data bytes occurring in a block stored from M.L. 3001H & onwards. The Length of block is stored in M.L. 3000H. Stores the result in M.L. 3100H.(Mar-2002)

5) A hex number is stored at M.L. 3000H. Write an ALP to interchange it's digits. The new number is to be stored at M.L. 3001H. Add original number with new number & stores the result at M.L. 3010H.(Mar-2002)

6) Write an ALP to count the number of times the data ADH is found in a block of M.L. starting from 3000H.Length of block is stored in location 2FFFH. Stores the result in location 2000H (Mar-2002)

7) Write an ALP to shifts a 16-bit number stored in memory location C000H & C001H to left by 2 bits & stores the result in M.L C002H & C003H.
(Mar-2003)

8) Write an ALP to get the decimal sum of a series of numbers whose length is stored in M.L. C000H & the series itself starts from M.L. C001H. Stores the result at M.L. C050H & C051H. (Mar-2003)

9) Write an ALP to search for the 1st occurrence of data FFH in memory block 1050H to 1059H.If successful stores the address of the M.L. in HL rp, else stores 0000H in M.L. (mar-2003)

10) Write an ALP to finds the largest number from a series of numbers whose length is stored in C00AH. And series itself begins from C000BH. Stores the result in M.L. C050H.(Mar -2003)

11) Write an ALP to finds the product of two numbers stored in M.L. C005H and C006H. Stores the result in M.L. C000H & C0001H.
(Mar – 2003)

12) Write an ALP to find how many times data ABH appears in a memory block 1050H to 1059H. Stores the count in register C (Mar-2003)

13) Write an ALP to copy a block of data having starting address 8900H to the new location starting from 9100H. The length of block is stored at ML 88FFH.(Oct-2003)

14) Write an ALP to add two 8-bit BCD numbers stored at ML 5000H and 5001H. Stores the result at ML 5002H onwards starting with LSB.(Oct-2003)

15) Write an ALP to find out 2's compliment of five numbers stored from ML 3330H and onwards. Stores the result from ML 4100H. (Oct-2003)

16) A block of data is stored in ML from 9101H to 91FFH. Write an ALP to transfers the block in reverse order to ML 9200H & onwards. (Oct-2003)

17) Write an ALP to count the number of odd data bytes occurring in a block starting from ML address 7501H ?& 75FFH. Stores the result at ML 7600H.

18) Write an ALP to perform the multiplication of two 8-bit numbers where multiplicand is stored at ML 2501H & 2502H & multiplier is stored at 2503H.The result is to be stored at ML address 2504H & 2505H. (Note 8-bit multiplicand is extended to be 16-bit) (Oct-2003)

19) Write an ALP to divide a hexadecimal number stored in a ML 8000H by a hexadecimal number stored in ML 8001H. Stores the quotient at ML 8002H and remainder at ML 8003H. (M-2004)

20) An 8-bit number is stored in ML C400H. Write an ALP to count the 'zero' in the given number. Stores the count in ML C500H. (Mar-2004)

21) Write an ALP to transfer first 10 bytes of memory block starting from 5000H to a new block starting from 5020H (Mar-2004)

22) Write an ALP to generate the Fibonacci series for first eight numbers. Stores the series in a memory block starting from C100H. (Mar-2004)

23) The two BCD numbers are stored at ML 3400H & 3401H. Write an ALP to add these BCD numbers & stores the result in ML 3402H & 3403H.
(Mar-2004)

24) Write an ALP to count the occurrences of the data 9CH in a memory block starting from ML 4000H to 400FH. Stores the count at ML 4500H.
(Mar-2004)

25) Two three-bytes numbers are stored in BCD and EHL registers. Write an ALP to finds their sum & stores the result in EHL. (Oct-2004)

26) Write an ALP to divide data at location 1050H by data stored at location 1051H. Stores the quotient & remainder in 1060H & 1061H MLs respectively? (Oct-2004)

27) The length of block is in ML 1070H & block itself begins from 1071H. Write an ALP to stores the count of odd numbers in register C. (Oct-2004)

28) Write an ALP to transfer a block of data from ML 1050H to 1059H to ML whose address is 1070H using XCHG instruction (Oct-2004)?

29) Write an ALP to finds the 2's compliment of a sixteen bit numbers, stored in ML C000H & C001H. Stores the result in ML C002H & C003H?
(Oct-2004)

30) Write an ALP to check validity of a given code at ML C020H. A code is said to be valid, if count of high i.e. logic 1 in first five MSB's reads two & remaining three bits reads low i.e. logic 0. If code is valid then HL should reads AAAAH or else it should reads FFFFH. (Oct- 2004)

31) Write an ALP to count the number of times a data D5H is found in a block of memory having starting address 3000H. Length of the block is stored in 2FFFH. Stores the result in ML at 2000H
(Mar-2005)

32) Write a program in assembly language to finds the product of two numbers stored in ML C005H & C006H. Stores the result in C000H and C001H.
(Mar-2005)

33) Write an ALP to get a decimal sum of a series of numbers whose length is stored in C000H & series itself starts from C001H. Stores the result in ML C050H & C051H? (Mar-2005)

34) Write an ALP to finds the smallest number from a series of numbers whose length is stored in C000H & the series itself begins from C001H. Stores the result in ML c050H? (Mar-2005)

35) Write an ALP to count the number of odd data bytes occurring in a block. Starting from ML 7501H to 75FFH. Stores the result at ML 7600H?
(Mar-2005)

36) A block of data is stored in memory from D001H. The length of block is stored in D000H. Another block of same length is stored from D101H. Write a program in ALP to exchange the contents of these two blocks (Mar-2005)

37) Write an ALP to separates two nibbles of an 8-bit number stored in ML 1500H. Add these two nibbles & stores the sum in memory at BABAH?
(Oct-2005)

38) Write an ALP to converts the given 8-bit number is stored in ML ABCDH into ASCII format & stores the ASCII value at ML ABCEH and ABCFH?
(Oct-2005)

39) Wire an ALP to perform the addition of 06H data to accumulator if auxiliary carry flag is set. Stores this sum in memory at BABAH? (Oct-2005)

40) Write an ALP to checks the validity of each number of the given series. The series is stored in ML starting from ABCDH to ABDDH. A number is said to be valid if 4 LSB's are greater than 4 MSB's. If the number is valid then stores 11H on that location, otherwise stores 00H on the same location
(Oct-2005)

41) A set of data bytes are stored in memory starting from ABCDH. Write an ALP to add 2-bytes at a time & stores the sum in the same ML low order sum replacing the 1st byte carry replacing 2nd byte. If any pair does not generates a CY, then the ML of second byte should be cleared? (Oct-2005)

42) Write a subroutine labeled "FIND" to searches the largest element from a given unsigned series stored in ML from ABBAH to ABCDH. Stores the largest element at ABCEH & its address in HL register pair? (Oct-2005)

43) Write an ALP to add all even numbers stored in a memory block of 10 locations is starting from 2000H. Stores the 2-byte sum at ML starting from ML 3000H(Mar-2006)

44) Write a program to set the sign & zero flag bits of the flag register to '1' & resets to '0' the remaining flag bits, The contents of an accumulator should be AAH. Also the content of BC,DE and HL rp should be same as that of PSW? (Mar-2006)

45) Write an ALP to fill up the memory bloc of 20 MLs starting from ML 2000H, with data bytes 00H and FFH, at every alternate MLs? (Mar-2006)

46) A three byte number is stored in a memory with starting address 2000H. Write a program to checks whether it is palindrome or not. If it is palindrome then it stores 00H in register B else it stores FFH? (Mar-2006)

47) Write an ALP to separates the nibbles of a number stored at ML 2000H. Multiply the separated nibbles & stores the result at ML 3000H?
(Mar-2006)

48) A BCD no. is stored at ML 2000H. Write an ALP to converts it into hexadecimal number & stores it is the next ML (Mar-2006)

49) Write an ALP to add all odd numbers stored in memory block of 10 locations starting from 2000H. Stores the 2-byte sum at MLs starting from 3000H? (Oct-2006)

50) Write an ALP to finds the sum of first 10 numbers of the series 2^0,2^1, 2^2,-------. Stores the two-byte result at MLs stating from address 2000H?
(Oct-2006)

51) Write an ALP to finds the occurrences of numbers divisible by 4 in a memory block of 10 locations starting from 2000H. Stores the count of occurrences at the end of block? (Oct-2006)

52) Write an ALP to generates the 1st ten numbers of Fibonacci series & stores them in a memory block starting from 2000H? (Oct-2006)

53) An ASCII code for a hexadecimal digit is stored at ML 2000H. Write an ALP to converts it into a hexadecimal number & stores it at ML 3000H.
(Oct-2006)

54) Write an ALP to count the number of 1's and 0's in a 8-bit binary number stored at ML 2000H. Stores the count for 0's and 1's in a memory location 2001H and 2002H respectively? (Oct-2006)

55) Write an ALP to shifts 16-bit number by three bit left stored in ML starting from BABAH with LSB. Stores the result starting from BADAH. (Mar-2007)

56) Write an ALP to sorts 25 numbers in ascending order stored in ML from AB01H & onwards. Stores the sorted data in memory from BC01H & onwards? (Mar-2007)

57) Write an ALP to finds greatest & smallest from a given series stored in ML from BABAH to BADAH. Stores the smallest number at BADBH & the greatest number at BADCH? (Mar-2007)

58) Write an ALP to fill the ML starting from AB00H & onwards with decimal number from 0 to 99? (Mar 2007)

59) Write an ALP to add two 8-bit numbers stored in ML ABCDH & ABCEH. Stores the sum in memory at ABDDH and the flag status at location ABDCH?
(Mar-2007)

60) Square of decimal numbers from 0 TO 9 are stored in memory from 1500H to 1509H respectively. Write an ALP to find the square of a given decimal number by lookup table method given in the above range & is stored at 14F2H. Stores the square of given number in memory at 14F3H?
(Mar-2007)

61) Write an ALP to count number of odd data bytes in a block of memory starting from ML 1300H to 13FFH & output on port 11H (Oct-2007)?

62) Write a program segment using appropriate 'Rotate' instruction to divide the number in BC rp by 2. The quotient should remains in BC rp?(Oct-2007)

63) Write an ALP to count how many times 05H comes in memory block starting at 4000H to 40004H. Stores the result at 4070H? (Oct-2007)

64) Write a program segment to finds the largest number in a series. The length of the series is stored at 2500H & the numbers are stored from 2501H. Stores the result at 2405H? (Oct-2007)

65) 16 bytes of data are stored in MLs at C050H to C05F. Transfers the entire block of data to a new ML starting at C070H? (Oct-2007)?

66) Trace the following program & wire the purpose of the program: (Oct-2007)

```
LXI H , 25000H
MVI B,01H
MOV A,M
CMA
ADD B
INX H
MOV M,A
HLT
```

67) Write an ALP to copy a block of data having starting address 2000H to a new destination with starting address 3000H. The length of the block is stored at 1FFFH. (Mar-2008)

68) A block of data is stored in memory as starting from ML D001H. The length of the block is stored at ML D000H. Write an ALP to sorts the contents of block in ascending order(Mar-2008)

69) Write an ALP to exchange the two hexadecimal digits of a number stored at ML 25000H. Stores the new number at ML 2501H.(Mar-2008)

70)Write an ALP to perform the multiplication of two 8-bit numbers where multiplicand is stored at ML 2501H and 2502H. The multiplier is stored at ML 2503H. the result is stored at ML 2504H & 2505H? (Mar-2008)

71) A block of data is stored in MLs from C080H. Length of a block is stored at C07FH. Write an ALP that searches for the first occurrences of data byte ABH in the given block. Stores the address of the occurrences in HL rp. If number is not found then HL rp must contains FFFFH? (Mar-2008)

72) Write a sub-routine to fill the MLs 2800H to 28FFH with the hexadecimal numbers 00H to FFH respectively? (Mar-2008)

73) Write an ALP to finds how many times the data BCH appears in a memory block D050H to D059H. Stores the count in register C (Oct-2008)

74) Write an ALP to finds the largest number in a block of data starting from the address 3500H. The length of the block is stored at ML address 34FFH. Stores the result at address 4500H? (Oct-2008)

75) Write an ALP to add two BCD numbers stored at locations 3500H & 3501H. Place the BCD result in location 3502H & onwards with LSB first? (Oct-2008)

76) Write an ALP to subtracts the number stored in ML 3601H from the number stored in ML 3600H. Stores the +ve result at location 3602H? (Oct-2008)

77) Write an ALP to divide a data byte stored at location 2050H by a non-zero byte stored at location 2551H. Place the quotient at ML 2552H & the remainder at location 2553H? (Oct-2008)

78) Write an ALP to transfer a block of data stored in ML from D100H to D1FFH in reverse order in new ML starting at D200H? (Oct-2008)

79) A block of data is stored in MLs from 8101H to 81FFH. Write an ALP to transfer the block in reverse order to MLs 8200H & onwards? (Mar-2009)

80) Write an ALP to count the number of even data bytes occurring in a block starting from the ML 7501H to 75FFH. Stores the result at ML 7600H? (Mar-2009)

81) Write an ALP that divides two 1-byte hex numbers where dividend is stored in MLs 8000H & divisor is stored in ML 8001H. Stores the quotient & remainder in MLs 8002H & 8003H respectively? (Mar-2009)

82) Write an ALP to exchange 8-bit number stored in ML 4000H. Stores the new number at ML 4001H? (Mar-2009)

83) Write an ALP to separates the nibbles of a number stored at ML 4000H. Multiply the separated nibbles & stores the result at ML 5000H? (Mar-2009)

84) Write an ALP to subtracts the number stored in ML ABB8H from the number stored in ML ABB7H. Stores the +ve result at ML ABB9H? (Mar-2009)

85) Write an ALP to find greatest number among a content of block of memory which starts from D001H, the length of block is stored at D000H. Stores the greatest number at the end of the block? (Mar-2010)

86) Write a program in assembly language to sum the series, stored from D001H, length of series is at D000H. Stores the result from D100H? (Mar-2010)

87) Write a program in assembly language to subtract content of memory location D001H from the contents of ML D000H. Stores an absolute difference at D002H? (Mar-2010)

88) Give appropriate comment to the following program:

Label	Mnemonics	Comments
	STC ;	_____
	CMC;	_____
	MVI A,08H;	_____
	MVI C, 0AH;	_____
	LXI H, D001H;	_____
LOOP:	MOV M, A;	_____
	INX H;	_____
	DCR C;	_____
	JNZ LOOP;	_____
	HLT;	_____

89) Trace the following program and show contents of the following by filling blanks:

Label	Mnemonics
	MVI A, 05H
	LXI H, D001H
	MVI C, 05H
LOOP	MOV M , A
	DCR A
	INX H
	DCR C
	JNZ LOOP
	HLT

Mar (2010)?

[D005] = _____

[A] = _____

[C] = _____

Reg. H = _____

Reg. L = _____

90) A series of numbers are stored in memory locations from C001H to C008H.Write a program in assembly language to find largest number among these numbers. Store largest number in memory location C009H.(Oct-10)

91) Write an assembly language program to count number of times the data A4H is found in a block of memory location starting from 4000H. The length of block is stored in location 3FFFH. Store result in location 5000H. (Oct-10)

92) Write an assembly language program to fill memory locations 3000H to 30FFH with the hexadecimal numbers 00H to FFH respectively. (Oct-10)

93) Write an assembly language program to copy a block of data having starting Address 7900H to the new location 9100H. The length of block is stored at memory location 78FFH. (Oct-10)

94) A block of data is stored in memory locations from D001H. The length of block is stored in occurrence of data 11H in given block. Store address of this occurrence in HL pair. If the number is not found then HL pair should contain 0000H. (Oct-10)

95) A hex number is stored at location C000H. Write an assembly language program to interchange its digit. The new number is to be stored at C001H. Add original number with new number and store result at location C010H. (Oct-10)

96) Write an Assembly Language Program to add all odd numbers stored in memory block of 10 locations starting from 2000H. Store two byte sum at memory location starting from 3000H.(Mar-11)

97) Write an Assembly Language Program to separate nibbles of a number stored at memory location 2000H. Multiply separated nibbles and store result. (Mar-11)

98)Write a program in Assembly Language Program to transfer a block of data from 1050H to 1059H to memory location whose starting address is 1070H. (Mar-11)

99) Write an Assembly Language Program to count number of even data bytes occurring in a block starting from memory location C030H to C039H. Store result at the memory location C040H. (Mar-11)100) Write an Assembly Language Program to exchange position of digit of number stored at C040H. Multiply original number with the exchanged number the result to be stored at memory location starting from C041H and onwards. (Mar-11)101) Write an Assembly Language Program to add two 16 bit numbers. The numbers are stored at memory location C030H and C031H and the second number stored at C032H and C033H. Store result at memory location C034H and C035H. Store final carry at C036H. (Mar-11)

102) Write a program in assembly language to find the position of a data 05H in a block of memory D001H to D005H. If data is found then store the position of data at memory location D100H else store 00H at the same memory location.
(Note : It is assumed that data 05H may present only at once.) (Oct-11)

103) Write a program in assembly language to double the contents of block of memory from D001H to D00AH. Store the doubled contents at same memory locations.
(Note: It is assumed that contents are not exceeding 0FH.) (Oct-11)

104) Write a program to exchange the two nibbles stored at 2500H. Store the exchanged number at 2501H. (Oct-11)

105) Write a assembly language program to copy the contents of a block of memory which is from 2501H to 2505H to another block begins from 3501H.
(Oct-11)

106) There are two blocks of memory one is from 2501H to 2505H. Another is from 3501H to 3505H. Write a program in assembly language to check whether contents of these two blocks are exactly same or not. If contents are same then memory location D100H should contains 00H else FFH. (Oct-11)

107) Write a program in assembly language to check whether contents of these two blocks are exactly same or not. If contents are same then memory location D100H should contains 00H else FFH.
(Oct-11)

108) Write a program in assembly language to rotate the content of memory location D000H towards left by one bit position and add original contents with rotated number and store the result from D001H. (Oct-11)

109) An 8-bit number is stored in memory location 4400H. Write an assembly language program to count ‘zero’ in the given number. Store count in memory location 4500H.
(Mar-12)

110) A series of numbers are stored in memory locations from C001H to C008H. Write a program in assembly language to find smallest number among these numbers. Store smallest number in memory location C009H. (Mar-12)

111) Write an assembly language program to count number of odd data bytes occurring in a block starting from memory location A001H to A0FFH. Store result at memory location B000H. (Mar-12)

112) A hex number is stored at location AB00H. Write an assembly language program to interchange its digit. The new number is to be stored at AB01H. Add original number with new number and store result at location ABCDH. (Mar-12)

113) Write an assembly language program to add two BCD numbers stored at locations AB00H and AB01H. Place BCD result in location AB02H and onwards starting with LSB. (Mar-12)

114) Write a program in assembly language to find 2's compliment of 8bit number stored in memory location C000H. Store result at memory location C001H. (Mar-12)

115) Write an ALP to subtract the number stored in memory location 3601H from the number stored in memory location 3600H. Store the positive result at location 3602H.(Oct-12)

116) Write an ALP to generate the Fibonacci series for first eight number. Store the series in a memory block starting from C100H. [Note : The first eight numbers of series are : 00, 01, 01,02,03,05,08,0D] .(Oct-12)

117) Write an Assembly Language Program to multiply the given BCD data at location C050H and C051H. Store the result in C060H and C061H respectively.(Oct-12)

118) Write a program in assembly language that converts a BCD number stored at C030H to its hexadecimal equivalent. Store the hexadecimal result in C031H.(Oct-12)

119) Write an ALP to count number of even data byte occurring in a block stored from memory location 3001H and onwards the length of block is stored in location 3000H store the result in 3100H.(Oct-12)

120) Write an Assembly Language Program that multiplies the original number. Stored at C030H with its lower nibble. Store the result starting from C031H and onwards.(Oct-12)

121) Write assembly language program to count number of even data bytes occurring in a block stored from memory location C051H and onwards. The length of block is stored in location C050H. Store result in location C060H. (Mar-13)

122) Write an assembly language program to perform multiplication of two 8bit numbers where multiplicand is stored at the memory locations C051H and C052H and multiplier is stored at C053H. The result is to be stored at memory location address C054H to C055H. (Note: 8-bit multiplicand is extend to 16-bit). (Mar-13)

123) A hex number is stored at location 3000H. Write an assembly language program to interchange its digits. The new number is to be stored at 3001H. Add original number with new number and store result at location 3010H. (Mar-13)

124) Write assembly language program to count occurrences of the data ABH in a memory block is starting from 4000H to 400FH. Store count at memory location 4500H. (Mar-13)

125) A block of data is stored in a memory location from 7500H to 75FFH. Write an assembly language program to transfer block in reverse order to memory location 7600H and onwards. (Mar-13)

126) Write an assembly language program to find largest element in a block of data. The length is in memory location D000H and block begins in memory location D002H. Store maximum in D000H. Assume that all number are 8 bit unsigned binary numbers. (Mar-13)

127) Write an Assembly Language Program to count the number of times data 7EH is found in a block of memory location starting from 3000H. Length of block is stored in location 2FFFH. Store the result in location 2000h.(Oct-13)

128) Write a program in Assembly Language that multiply two 8-bit numbers stored in memory location D000H and D001H. Store the two byte result in consecutive memory locations starting from D002H. (Oct-13)

129) Write a program in Assembly Language that converts a hexadecimal numbers stored at C030H to its BCD equivalent. Store the BCD result in C031H onwards (AFH=0175 BCD). (Oct-13)

130) Write an Assembly Language program that divides two one byte hex numbers where dividend is stored in memory location C000H and divisor is stored in memory location C001H. Store quotient and remainder in memory location C002H and C003H respectively. (Oct-13)

131) Write an ALP to calculate sum of series of

Label	Mnemonics+Operand	Comment/Remark
	MVI C, 0AH	;
	MOV A, C	;
	RRC	;
	MOV C, A	;
	LXI H, D000H	;
	LXI D, D00AH	;
L1	LDAX D	;
	MOV B,M	;
	XCHG	;
	MOV M, B	;
	STAX D	;
	XCHG	;
	INX H	;
	DCX D	;
	DCR C	;
	JNZ L1	;
	HLT	;

number. The length of the series is in memory location C100H and series itself begins in memory location C101H. Assume sum to be an 8-bit number. Store result in C204H. (Oct-13)

132) An Assembly Language Program to find 2's complement of five numbers stored from memory location C030H and onwards. Store the result from memory location D000H. (Oct-13)

133) Write an ALP to store 00H in register B only if the contents of memory location 201FH is odd. Otherwise store EEH in register B. (Mar-14)

134) Write ALP to find largest element in a memory block from D000H to D00FH**.** Stores largest number at memory location C800H. (Mar-14)

135) Write an ALP to add all the BCD numbers in a block from 2001H to 2009H. Store SUM at memory location 200AH. (Assume SUM is 8 bit). (Mar-14)

136) Write an ALP to find SUM of a number and its reverse which is stored at memory location 2080H. Store SUM at 2081H. (Mar-14)

137) Write an ALP to count total number of occurrences of data 9CH in a memory block of length 16 byte, starting from 1000H. Store count in register E. (Mar-14)

138) Write an ALP to copy 10 consecutive bytes from memory 2025H to memory locations BCBCH and onwards. (Mar-14)

139) Write a program in assembly language to multiply two 8-bit data, where multiplier is stored at D000H and multiplicand is stored at D001H memory locations. Store the 16 bit product from memory location D002H. (Oct-14)

140) Give proper comments to following program. Also write the purpose of Program. (Oct-14)

141) There is a block of memory from 2501H to 250AH. Write a program to replace the odd numbers with data 'FFH' in a given block. (Oct-14)

142) Write program in assembly language to exchange the nibbles of each memory location contents of a block which begins from 2501H the length of block is at 2500H. Store the result at same memory locations. (Oct-14)

143) Write a program to check whether 2 hex digits stored at D000H are same or not. If digits are same then memory location D001H should contain 00H else FFH. (Oct-14)

144) Write a program in assembly language to add 3 byte number stored from D000H with another 3 byte number is stored from D100H memory address. Store the 3 byte result from memory location D200H starting with lower Byte. (Oct-14)

145) Write an ALP to multiply number stored at 8085 by 09H and store result at 8086H and 8087H with lower byte at 8086H. (Mar-15)

146) Write an ALP to find 2's compliment of a 16-bit number in DE pair. Store result in HL pair. (Mar-15)

147) Locate smallest number in a block from 2050H to 2060H and store it in memory location 2061H. (Mar-15)

148) Write an ALP to store data BCH in 20 contiguous memory locations starting from 8081H. (Mar-15)

149) Write an ALP to divide number at 6068H by a non-zero number at 6067H. Store quotient at 6069H and remainder at 606AH. (Mar-15)

150) Write an ALP to clear register B if number at memory location 20F9H is Palindrome; otherwise store FFH in register B. (Palindrome numbers such as FFH, 22H, AAH etc.) (Mar-15)

151) Write an assembly language program to multiply the content of 2000H by the content of 2001H. Store the 16-bit result in the memory location 2010H and 2011H. (Oct-15)

152) Write an assembly language program to add the four byte number starting from C000H with another four byte number starting from C100H. Store the four byte result starting from C200H and carry at C204H. (Oct-15)

153) Write an assembly language program to count the odd numbers block starting from 2300H to 2320H. Store he count at memory location 2400H. (Oct-15)

154) The two memory block starts from 3000H and 3100H each containing 16 bytes. Write an assembly language program to exchange the content of these blocks. (Oct-15)

155) A memory block from 4000H containing 16 hexadecimal numbers. Write an assembly language program to count the numbers which has identical nibbles. Stores the count in memory location 4010H. (Oct-15)

156) Write an assembly language program to test whether the DCH is present in the memory block which starts from 2000H. If the data is present in block then HL pair should contain the address otherwise it should contain FFFFH. (Test for the first occurrence only). (Oct-15)

157) Write an Assembly Language Program to multiply a number stored at location 1050H with a number at location 1051H. Result is 2-byte. Store result at locations 1052H and 1053H. (Mar-16)

158) Write an Assembly Language Program to transfer a block of memory starting from 1050H to a new location starting from 1070H to 1079H. (Mar-16)

159) A two byte number is stored at location C000H and C001H. Write an ALP to rotate this number to left side 3 places and store the rotated number in BC register pair. (Mar-16)

160) Write an Assembly Language Program to add 2 decimal numbers stored at 1050H and 1051H. Store result at 1052H and 1053H. (Mar-16)

161) Accumulator contents of 8085 are B7H and register B contents are A5H. What will be the effect of following instructions on the contents of Accumulator when executed following instructions independently? i) ADI 05H ii) CMP B iii) CMA iv)XRA B v) ORA B (Mar-16)

162) Write an Assembly Language Program to increment the contents of alternate memory locations each by two from 1051H to 1060H. (Mar-16)

163) Write an Assembly Language Program to add the content of a block of memory comprising of 16 bytes, starting from 2000H. The two byte sum is to be stored in memory location 2010H (LSB) and 2011H(MSB). (July-16)

164) A memory block starts from 2100H and end at 210EH. Write an Assembly Language Program to insert a byte 2CH at memory location 2105H and rearrange the memory block accordingly. (July-16)

165) Write an Assembly Language Program to find the absolute difference of the hex numbers stored at C200H and C201H. Store the result at C202H. (July-16)

166) A memory block starts form C301H and its block length count is stored at C300H. Write an Assembly Language Program to count the even numbers and odd numbers present in the block. Store the even number count at C400H and odd number count at C401H. (July-16)

167) Write an Assembly Language Program to separate the digits of a hex number stored at 2400H. Add these digits and store the sum at 2401H. (July-16)

168) Write an Assembly Language Program to pickup the largest number from a memory block starting from D000H containing twenty numbers. Store the largest number at D050H. (July-16)

169) Write a Assembly Language Program to copy a block of data having starting address 4500H to new location starting from 4600H. The length of block is stored at memory location 44FFH.(Mar-17)

170) Write an Assembly Language Program to add two 8-bit BCD numbers stored at memory location 4500H and 4501H. Stores the two byte BCD result from memory location 4502H and onwards. (Mar-17)

171) Write an Assembly Language Program to fill the memory locations 4500H to 4504H with hexadecimal numbers 09H to 0DH respectively. (Mar-17)

172) Write an Assembly Language Program to exchange the nibbles of 8-bit number stored in memory location 4500H. Stores the result at memory location 4501H. (Mar-17)

173) A block of data is stored in memory location 4500H. The length of block is stored in memory location 44FFH. Write an Assembly Language Program that searches for the first occurrences of data D9H in given block. Store the address of this occurrence in HL pair. If the number is not found the HL pair should contain 5000H. (Mar-17)

174) A block of data is stored from memory location 4501H and onwards. The length of the block is stored at memory location 4500H. Write an Assembly Language Program to find the sum of block of data. Store the two byte result From memory location 4600H. (Mar-17)

175) Write an Assembly Language Program to fill the memory block stored from 7601H to 760FH with the data 00H and FFH alternatively. (July-17)

176) Write an Assembly Language Program to search the data byte A4H in a memory block stored from 9901H to 990AH. If the search is successful, then HL register pair should contain the address of the location where the specified data byte is found; else the HL pair should contain 0000H. (July-17)

177) Write an Assembly Language Program to separate the two nibbles of an 8-bit number stored at 7501H. Store the low-order nibble and high-order nibble respectively at the locations 7502H and 7503H. (July-17)

178) Write an Assembly Language Program to take the sum of the 8-bit contents of a memory block stored from 2201H to 220AH. Store the 2-byte result at the locations 220BH and 220CH starting with LOB (Lower-Order byte) (July-17)

179) Write an Assembly Language Program to count the total number of 0(LOW) bits in an 8-bit number stored at the location 4301H. Store the result(count) at the memory location 4302H. (July-17)

180) Write an Assembly Language Program to find the greatest number in a memory block stored from 6201H to 620AH. Store the result at the location 620BH. (July-17)

181) Write an Assembly Language Program to multiply an 8-bit number stored at 4301H by another 8-bit number stored at 4302H. Store the result at the location 4303H and 4304H beginning with LOB(Lower Order Byte).(Mar-18)

182) Write an Assembly Language Program to fill in the memory locations starting from 6900H and onward with the decimal numbers 0 to 99. (Mar-18)

183) Write an Assembly Language Program to take the 2's compliment of an 8-bit number stored at 3301H. Store the result at the memory location 3302H. (Mar-18)

184) Write an Assembly Language Program to count the occurrence of the data byte ACH in a memory block stored form 7401 to 7405H. Store the count at the memory location 7406H. (Mar-18)

185) Write a subroutine in assembly language to till the memory locations 7301H to 73FFH with the hexadecimal numbers 01H to FFH respectively. (Mar-18)

186) Write an Assembly Language Program to count the total number of even data bytes occurring in a block of data stored from 9201H to 920AH. Store the result (count) at the memory location 9500H. (Mar-18)

187) Write an Assembly Language Program to add two 16-bit numbers. The numbers are stored at memory location C030H and C031H and the second number is stored at C032H and C033H. Store result at memory location C034H and C035H. Store final carry at C036H.(Aug-18)

188) Write the appropriate instructions for the following task: (Aug-18)`

i) Load accumulator from B register. **ii)** Complement the accumulator. **iii)** Add 01H with the accumulator.

iv) Store the content of accumulator at the memory location addressed by the BC register pair.

v) Clear the accumulator.

189) A block of data is stored in memory location from 9101H to 91FFH. Write an Assembly Language Program to transfer the block in reverse order to memory location 9200H and onwards. (aug-18)

190) Trace the following program and write the purpose of the program: (Aug-18)

Label	**Instructions**	**Comments**
	LXI H, 2500H	; Load HL by 2500H.
	MVI B, 01H	; Load immediate register B by 01H.
	MOV A, M	; Take data from memory to accumulator.
	CMA	; complement the accumulator content.
	ADD B	; Add 01H to accumulator.
	INX H	; Increment HL by 1.
	MOV M, A	; Transfer content of accumulator to memory.

Instruction set and programming of 8085 microprocessor

Aug-18	Explain conditional CALL and unconditional JMP instructions. (Any three each) .
Aug-18	Accumulator contains data 45H and register B contains data 82H. What will be the result in Accumulator after execution of each instruction independently. i) XRA B ii) ADI 54H iii) ANI 57H
Jul-17	Accumulator contains data A4H and register E contains data 69H. Write the contents of an accumulator in hex digits after execution of each of the following instructions independently: i) ANA E ii) CMP E iii) ORA E
Mar-14	Accumulator content is B8H and register B contents is C9H. What are the contents of accumulator and flag register after execution of instructions ANA B and SUB B independently.
Oct-13	Define addressing mode of 8085 and explain any two of them with example.
Mar-10	Describe the following instruction of 8085 Microprocessor : i) SPHL ii) XTHL iii) LXI rp
Oct-13	Differentiate between PUSH and POP.
Oct-13	Differentiate DAD and ADD instruction of 8085 Microprocessor.
Mar-13	Explain any three addressing modes of 8085 microprocessor with an example of each.
Mar-11	Explain any three addressing modes of 8085 Microprocessor with example.
Mar-16	Explain any three addressing modes of 8085 with examples.
Aug-18	Explain any three instructions of logical group of 8085 Microprocessor.
Oct-13	Explain conditional and unconditional RET instruction of Microprocessor 8085.
Mar-18	Explain direct and immediate addressing modes of Intel 8085 with suitable examples.
Oct-12	Explain following instruction of 8085 Microprocessor: i) SHLD ii) ORI iii) SBB
Oct-12	Explain following instruction of 8085: i) CPI data(8bit) ii) RAL iii) DAD rp
Mar-14	Explain Immediate and Implied Addressing Modes of 8085 MPU.
Oct-12	Explain PCHL instruction of microprocessor 8085 and justify the statement that it is equivalent to 3 byte unconditional jump instruction.
Mar-15	Explain PUSH and POP instructions of 8085.
Jul-17	Explain Register direct and Register indirect addressing modes of Intel 8085 with suitable examples.
Oct-14	Explain register indirect and immediate addressing mode with one example of each.
Jul-16	Explain register indirect and immediate addressing modes of 8085 microprocessor with one example of each.
Mar-10	Explain SIM instruction of 8085 in detail.
Mar-12	Explain stack operation in case of 8085 Microprocessor with the help of suitable instruction like PUSH and POP.
Oct-15	Explain the addressing modes of the following instructions of 8085 Microprocessor: i) STAX rp ii) CMA iii) LHLD addr
Mar-18	Explain the conditional CALL instructions of Intel 8085.
Oct-13	Explain the following 8085 instructions: i) XTHL ii) DAA
Oct-10	Explain the following 8085μP instructions with suitable example: i) SUI data ii) XRA M iii) LHLD addr
Oct-12	Explain the following instruction of 8085 : i) RLC ii) RAR with example

Mar-13	Explain the following instruction of 8085 microprocessor with suitable example of each : i) STA addr ii) ADD r iii) CMP r
Mar-13	Explain the following instruction of 8085 microprocessor with suitable example of each : i) XTHL ii) DAD rp
Oct-11	Explain the following instructions : i) LDA addr ii) LHLD addr iii) XRI data
Oct-14	Explain the following instructions of 8085 : i) EI ii) PCHL iii) POP rp
Mar-11	Explain the following instructions of 8085 Microprocessor : i) NOP ii) XRA reg iii) LHLD addr
Mar-17	Explain the following instructions of 8085 Microprocessor with one example of each : i) PUSH PSW ii) INX rp iii) DAD rp
Mar-12	Explain the following instructions of 8085 Microprocessor with suitable Example: i) DAA ii) DAD rp
Mar-12	Explain the following instructions of 8085 Microprocessor with suitable Example : i) SBB M ii) CPI data iii) XTHL

Instruction set and programming of 8085 microprocessor

Oct-10	Explain the following instructions of 8085 Microprocessor with suitable example : i) SPHL ii) PCHL
Oct-15	Explain the following instructions of 8085 Microprocessor with suitable example of each : i) LXI rp ii) XRA r iii) RLC
Jul-16	Explain the following instructions of 8085 Microprocessor with suitable example. i) XTHL ii) PCHL
Jul-16	Explain the following instructions of 8085 Microprocessor: i) LDAX rp ii) XCHG iii) DAD rp
Mar-15	Explain the following instructions of 8085 MPU. i) MOV B, M ii) ADC C iii) SPHL iv) XCHG
Oct-15	Explain the following instructions of 885 Microprocessor with suitable example of each : i) POP rp ii) SPHL
Mar-13	Explain the following instructions with diagram : i) RLC ii) RRC iii) RAL iv) RAR
Mar-18	Explain the function of following instructions of Intel 8085 : i) LXI H,2900H ii) LDA 6605H iii) PUSH B
Jul-17	Explain the function of following instructions of Intel 8085: i) DAD ii) RAL iii) CMC
Mar-12	Explain with suitable example of followings 8085 Microprocessor: i) Register Indirect addressing mode ii) Implied Addressing mode
Oct-10	Explain with suitable examples following addressing modes of 8085 µP: i) Implied ii) Register
Mar-11	If accumulator contains data ABH and C register contains data EFH, What will be the contents of accumulator after execution of the following instruction independently: i) ADD C ii) SUB C iii) ORA C

Oct-13	If accumulator contains the data 23H and B register contains 35H. What will be the contents of accumulator after execution of each of the following instruction independently: i) XRA B ii) ANI F0H iii) CPI 0AH
Oct-10	In case of 8085 microprocessor, explain unconditional & conditional branching instructions with suitable examples.
Mar-15	State any six Arithmetical and Logical Instructions of 8085 MPU.
Oct-12	State the number of bytes using and addressing modes of the following instruction of 8085 Microprocessor. i) LXI ii) STAX iii) IN
Mar-10	The accumulator contains data 05H and register B contains 08H. What will be the effect of 'SUB B' instruction on flags? Explain it with diagram.
Oct-14	The accumulator contains data 05H, register B contains data 08H. What will be contents of flags on execution of ADD B instruction.
Oct-14	The accumulator contains data 3CH, what will be the effect on its content if following instructions are executed independently : i) ANI 05H ii) RRC iii) MOV B, A
Jul-16	The accumulator in 8085 contains data AAH and register B contains 55H. What will be the contents of accumulator after execution of each of the following instructions independently. i) ADD B ii) ORA B iii) RRC
Mar-17	The accumulator in 8085 microprocessor contains data 71H and register E contains data 39H. What will be the contents of an accumulator in hexadecimal after execution of the following instructions independently? i) ADD E ii) ORA E iii) RRC
Oct-15	The accumulator in 8085 Microprocessor contains the data 78H and register D contains data 33H. What will be the content of accumulator after execution of each of the following instructions independently : i) SUB D ii) ANA D iii) CMA
Mar-12	The accumulator of 8085 contains data B7H. What will be its contents after execution of the following instructions independently : i) ORI 58H ii) CMA iii) ANI E3H
Oct-10	The accumulator of 8085 Microprocessor contains data F2H. What will be its content after the execution of the following instructions independently: i) XRI 3BH ii) RAL iii) SUI AEH
Mar-13	The accumulator of 8085 processor contains data B8H and register B contains 44H. What will be the content of accumulator after execution of each of the following instruction independently : i) ORI F0H ii) ANA B iii) XRI 0FH
Mar-18	The register A and C of 8085 contains the data E2H and 47H. What will be the contents of an accumulator in hex digits after execution of each of the following instructions independently? i) SUB C ii) XRA C iii) ADD C
Mar-11	What are the different ways of clearing accumulator (A=00H) in single Instruction?
Oct-11	What is a sub-routine? Give its related instructions in 8085.

Instruction set and programming of 8085 microprocessor

Oct-11	What is addressing mode? Identify the addressing mode of following 8085 instructions : i) MVI A, 05H ii) MOV A,B iii) CMA iv) STAX B

Mar-17	Write any three instructions to make accumulator zero.
Jul-17	Write appropriate instructions for each of the following tasks: i) Add contents of DE pair to HL pair. ii) Store the contents of Accumulator to memory location pointed by BC pair. iii) Rotate contents of Accumulator towards left with carry bit.
Mar-17	Write the addressing mode and length in bytes of the following instructions: i) CPI 10H ii) MOV M, B iii) SHLD C009H

CHAP : NETWORKING TECHNOLOGY

H.S.C. BOARD TOPIC WEIGHTAGE : 18 Marks

1 Mark obj	**= 1**	**= 1x1**	**= 01**
3 Mark que	**= 3**	**= 3x3**	**= 09**
4 Mark que	**= 2**	**= 4x 2**	**= 08**

Q1)What is computer n/w? What are advantages if computer n/w(s)
OR
What is n/w? What its goals?

A computer n/w may be described as the interconnection of two/more computer system by transmission media for the communication i.e. sharing of information and sharing of resources purposes.

Advantages/Goals of computer n/w:

1) N/W provides a very rapid method for sharing & transferring files and s/w(s).
2) N/W provides resource sharing the resources are either s/w or h/w.
3) N/W provides security for files and programs that means it protected from unauthorized sources.
4) N/W provides centralized s/w management i.e. all s/w(s) can be loaded on one computer called as file server.
5) The presence of n/w provides h/w necessary to install an email system.
6) N/W(s) allows authorized users to access their files from computers throughout the n/w organization.
7) N/W provides workgroup computing i.e. it allows many users to works on a document or project concurrently.

Disadvantages of N/W

1) Expensive to install cables, n/w cards and s/w are expenses and the installation may requires the services of a technician.
2) Proper maintenance of a n/w requires considerable time and expertise.
3) When file server of n/w is failure then entire n/w may come to halt.

Q2) What are different types of computer n/w(s)?
OR How computer n/w(s) are classified according to geographic locations?

The computer n/w are classified according to geographic location i.e coverage area and its facility as follows:

1) LAN (Local Area Network)
2) MAN (Metropolitan Area Network)
3) WAN (Wide area Network)

Local Area Network (LAN)	
Definition	The interconnection of more than one computer in a single room and rooms within a building or buildings on one site are called as LAN called as small size n/w.
Data Transfer Rate Or speed	Very Highest than all N/W is 10 MBPS TO 1 GBPS
Transmission Media used or link used	Co-axial cable and twisted pair cable is used to link or interconnects n/w
Max. Distance or Diameter	Upto 10 kms
Advantages	1) Due to short distance short circuit errors or noise are created minimum as compared to other n/w(s) 2) Reliability of this n/w is higher than all n/w(s)
Disadvantages	1) Limited geographic area for coverage. 2) No long communication system because small size n/w.
Examples	1) A n/w in LAB 2) A n/w in campus 3) A n/w in building

Metropolitan Area Network (MAN)	
Definition	The interconnection of many LANs in one city is called as MAN. This n/w is smaller than WAN but larger than LAN so it is called as medium size n/w.
Data Transfer Rate Or speed	Slower than LAN and faster than WAN.
Transmission Media used or link used	Fiber optic cables and microwave links are used for connecting n/w(s) i.e. interconnection of computers.
Max. Distance or Diameter	Upto 50 kms i.e it covers one city area.
Advantages	1) Coverage area larger than LAN. 2) Don't contains switching elements in n/w.
Disadvantages	Noise errors are maximum than LAN but small than WAN.
Examples	1) A n/w within city. 2) A n/w is receiving TV programs from satellite and connects to many users. 3) Pager system

Wide Area Network (WAN)	
Definition	The interconnection of many MANs on one site which covers nationwide or worldwide or state or country is called as WAN.
Data Transfer Rate Or speed	Very slow as compared to any n/w(s) is upto 1200 BPS TO 2 MBPS.
Transmission Media used or link used	Telephone cables, microwave towers and satellite are used for interconnection.
Max. Distance or Diameter	It covers number of cities, countries and world.
Advantages	1) Internet is accessible from this type of n/w. 2) No area limit for n/w coverage. 3) No extra physical link is required.
Disadvantages	1) Cost is higher than any n/w. 2) Noise is higher than any n/w. 3) Speed is very lower than any n/w.
Examples	1) National Telephone System 2) Cellular mobile phones. 3) Web site accessed from remote computer to any other computers.

Q) What is Transmission medium? Gives the transmission media characteristics?

The pathway through which individual systems are connected in a n/w are called as transmission media.

** Characteristics of Transmission Media:-

1) Cost:- While designing a n/w cost is determined. The cost is the one major factor in purchase decision of any networking component is its cost. The decision is depends upon whatever application and standard of resources etc used by user.

2) Installation Requirement:- According to actual physical layout n/w the raw fact which are need to build n/w is determined this is known as installation requirement.

3) Bandwidth : Bandwidth measure the capacity of a medium to transmit data. The bandwidth of cable is depends on cable length. A short cable have greater bandwidth while long cable have minimum bandwidth. Bandwidth of cable is measure in BPS.

4) BandUsage :- The method of division of bandwidth into one or multiple communication channel is known as bandusage.

Theses are categorized into two types as follows:

a) Base Band : Base band divides bandwidth into one communication channel on a available bandwidth. Base bands signals are either analog or digital. Original information is directly sent on line.

e.g LAN, telephone lines etc.

b) Broad Band : Broad Band divides bandwidth into multiple channels on available bandwidth.

e.g Cable TV channel transmission.

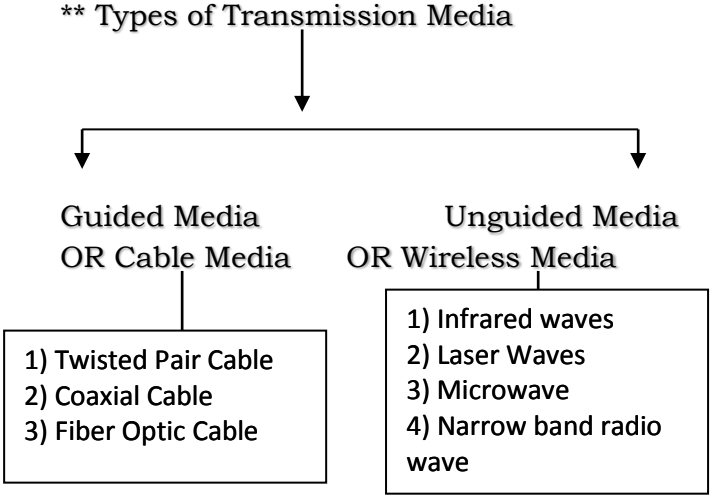
5) Attenuation : - Attenuation measures how much weak signals travels through a medium. As signal pass through the medium then part of the signal is absorbed and makes the signal weak. Attenuation also measures noise signal travels through a medium when signal strength falls below certain limits then at receiving station noise is appeared.

6) Immunity from electromagnetic interference (EMI) :-

An EMI is occurred when outside electromagnetic waves and also unwanted noise signals produced by various electrical appliances. EMI affects the signal which is transmitted through a media. The EMI affects is called either sensitive or less sensitive or free from EMI.

e.g. crosstalk is best example of EMI, it occurs when the signal from one wire is picked by another wire.

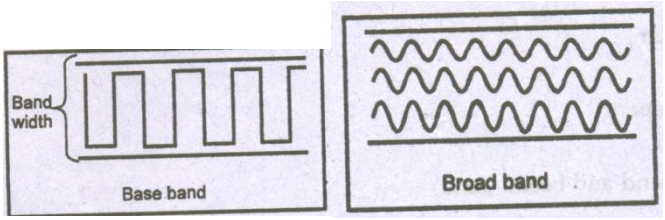
** Types of Transmission Media



Q) What is a difference between base band broad band of transmission medium characteristics?

OR Compare in between baseband and broad band

Baseband	Broadband
1)Only one communication channel is transmitted on available bandwidth.	1) Many/Multiple channels are transmitted on available bandwidth.
2) Original information is directly sent on line.	2) Information is modulated and indirectly sent in different form.
3) Small band width can be used.	3) Large bandwidth is required to transmit more channel.
4) e.g. LAN or a telephone line	4) e.g. Cable TV channel transmission
5) Twisted pair cable is used.	5) Co-axial cable is used



Q) What are the advantages of wireless transmission?

The following are advantages using wireless transmission:

1) High data rates by using large bandwidth.

2) Wireless medium can gives transmission speed around 24KBPS. 3) By this media the communication can reach rural and hilly areas.

4) Bandwidth for digital data is 1 To 10 MBPS.

5) Accessing the Internet using a cellular phone. 6) Establishing a home or business internet connection over satellite.

7) Beaming data between two hand-held computing devices.

8) Using a wireless keyboard and mouse for the PC.

Q) What are different wireless media?
OR State four types of LAN wireless transmission method? Describe in brief?

Wireless media name suggested that these are connectionless unguided media. The term unguided or unbounded media states that these are natural parts of the earth's environment that can be used as physical paths to carry electrical signals.

These media carries electromagnetic signals such as Infrared, Laser, Narrow-band radio and Microwave etc.

The n/w signals are transmitted through all transmission media as a type of waveform.

1) Infrared wave :

a) It is invisible band of radiation at the low frequency end of light spectrum.

b) In this transmission infrared rays are created when transmitter and receiver put along direct line of sight.

c) Used in only short range communications.

b) Maximum range upto 100 feet.

c) Bandwidth Theory rate is 10MBPS but 1-3MBPS is more typical.

d) examples: Remote of TV, In astronomy to detect stars it used, V.C.R. etc

2) LASER wave :

a) It is device for generating amplifying and concentrating light waves into an intense beam in one specific direction.

b) When transmitter and receiver in straight of sight towards each other then LASER rays are created.

c) This wave is used for LAN and WAN transmission.

d) examples: Laser printer, zerox machine

3) Narrow-band radio or radio waves

a) It is a wireless telegraphy on telephone.

b) A single frequency is used for transmission.

b) The range of this wave is greater than infrared wave.

c) The receiver and transmitter need not to put along with a direct line of sight. Because these are ominidirectional i.e this wave travels in all directions. Thus there is no need to place the receiver and transmitter along direction line of sight.

4) Microwave :

a) The microwave is an UHF i.e ultra high frequency section of the electromagnetic spectrum , which visible light.

b) A parabolic dish antenna can be used to focus the transmitted power into a narrow beam to gives a high signal to noise ratio. This antenna is place on local peak such as top of buildings or hill etc.

c) Microwave is used in many communication applications such as satellite, cellular phones ground communication etc.

d) Microwave are used for long distance communication

Q) What are applications using microwave ?
OR What are different forms of microwave?

Microwave technology has applications in all wireless n/w(s). Microwave communication can takes two forms such as below:

1) Terrestrial (ground) link
2) Satellite link

1) Terrestrial (ground) link:- In this communication the transmitter and receiver are earth based. The frequencies used are in low giga hertz. Telephone relay towers uses this type of communication.

This transmission is used for voice and television transmission and private communication and telephone n/w e.g. emergency services, utilities etc.

2) Satellite links: Typical use of satellite microwave is that in television-distribution, long distance telephone transmission, private business n/w(s) for global organizations etc. Because this satellite link uses point to point or broadcast transmission.

The satellite microwave system uses communication satellites. These are 22300 mils above the earth. It remains located at fixed point on earth. Earth stations uses satellite dishes to communicate with satellite. These satellite then transmits signal in narrow or broad beams, when destination is on opposite

side of earth then it may relay signal to another satellite.

Satellite links operates in low gigahertz range upto 11 to 14 GHz. Data rates are upto 1 To 10 MBPS. Attenuation depends on frequency power and atmospheric conditions. It is sensitive to EMI.

Q) State basic types of wireless n/w? How wireless n/w are useful in different situations or conditions?

There are three basic types of wireless n/w as mentioned below:

1) Wireless LAN: It contains one or more wireless n/w.

2) Extended LAN: A wireless connection between two LANs.

3) Mobile Computing: A mobile machine connecting to home n/w

*** Wireless n/w are useful in following situations:

1) Spaces where caballing is impossible. e.g. lobbies, older historical buildings, older buildings etc.

2)People who move around a lot in work area. e.g. doctors, administrators etc.

3) Temporary installations : To set temporary n/w that will be soon relocated.

4) Satellite offices, ships in ocean, teams in remote fields that need to be connected to main office.

Study of Transmission media:

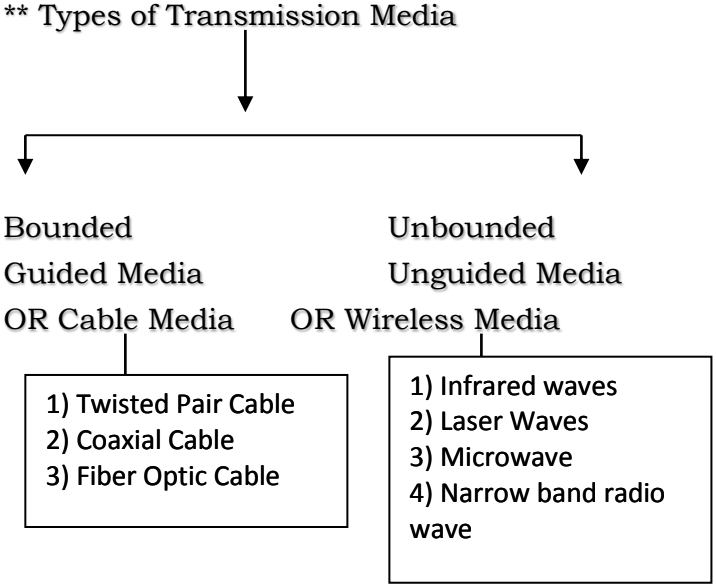
Q) What is transmission media? What its different types?

OR How transmission media are classified?

The pathway through which individual systems are connected in a n/w are called as transmission media.

Transmission media carries a signal between signal transmitter and signal receiver. These are electronic signal i.e. nothing but binary pulses(I/O) i.e. Input=ON and Output=OFF

** Types of Transmission Media



Q) What is Bounded OR Guided OR Cable Media? Explain in detail its types?

In this group media is used for short distance communication by laying a wire or cable hence called physical bounded media. Bounded media are also called cable media.

There are three types of cable media are available for communication as shown below:

1) Twisted pair cable

2) Coaxial cable

3) Fiber optic cable

Q) What is twisted pair cable? Describe in detail?

a) Twisted pair cable name suggested that two or more pairs of wires picked or twisted or bend on one another.

b) This is a guided or cable media generally is used to connects all nodes with different peripherals, which produces LAN..

**<u>Types of twisted pair:→</u>

There are two types twisted pair as below:

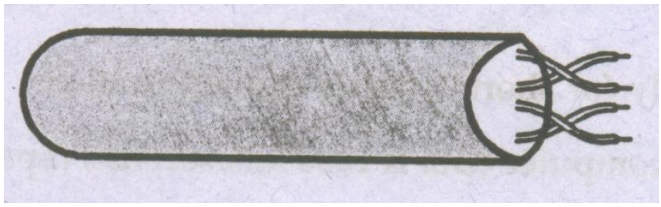
<u>1) UTP cable (Unshielded Twisted pair cable)</u>

The UTP does not have a braided shield into its structure. So that it is called as UTP i.e unshielded twisted pair.

** Uses of UTP

1) Used in to connecting nodes in LAN.

2) In telephone system it is generally used as a connecting medium.

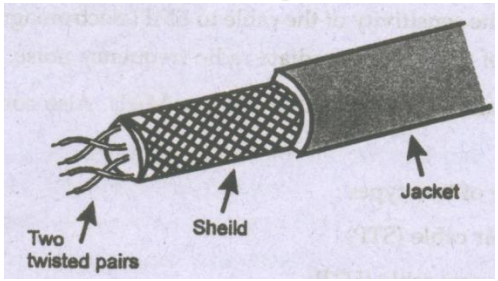


Characteristics of Unshielded Twisted Pair (UTP)

a) Cost :Lowest cost than all cable
b) Installation : very easy
c) Capacity : 100 MBPS
d) Range : 100 meter
e) EMI : Most sensitive because shield is not present so is present

2) STP cable (Shielded Twisted Pair cable)

STP so called because it contains shield i.e braided wires. The shield is connected to the ground portion of the electronic device to which cable s connected. The ground portion is a electrical reference point.



Characteristics of shielded Twisted Pair (STP)

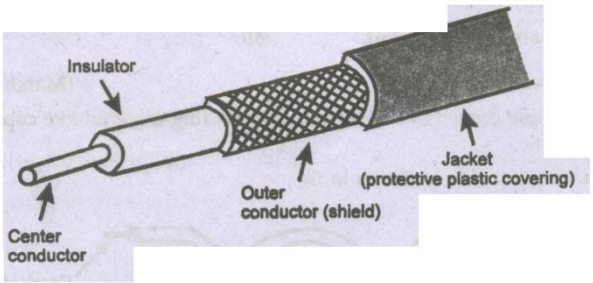
a) Cost : Greater than UTP and Coaxial cable but less than thicknet coaxial and fiber optic cable.
b) Installation : fairly easy depends on type of n/w
c) Capacity :
Theoretical-500MBPS
Practically-155 MBPS
d) Range : 100 meter
e) EMI : less sensitive and good EMI

Advantages of Twisted Pair:-→
1) This medium is inexpensive and easy to install.
2) Since wires are twisted it reduces EMI and also avoids RF radiation.
3) Twisted wires also reduce cross talk.

Disadvantages of Twisted Pair:→
1) They can be used only for short distance communications.
2) The twisted pair cable has limited bandwidth for audio telephone it is 4 KHz and it can be maximum 50 KHz.
3) The typical speed of computer data is 1200 bits/second (BPS).

2) Coaxial Cable :→

The coaxial name suggested that a common axis is shared by two conductors in transmission. The coaxial cable refers to a cable that has two or more conducting wires and each surrounding the one before through insulated from it. Such cables are generally used in LAN. Coaxial cable is quite common in connecting video equipments.



** Components of coaxial cable:->

The coaxial cable contains following types of components:

a) A center conductor:→

This is a solid copper wire or stranded wire.

b) An Outer Conductor:→

This forms a tube surrounding the centre conductor. This conductor is braided wires with metallic foils or both. The outer conductor is called as shield. The shield serves as a ground and protects inner conductor from EMI.

c) An insulator layer:→

This keeps outer conductor spaced evenly from the inner conductor.

d) A plastic jacket:→

This protects cable from damage from external environment.

Types of Coaxial Cable:→

There are two types of coaxial cable as shown below:

1) Coaxial Thinnet:- It thin i.e. flexible cable than thicknet coaxial and inexpensive than thicknet coaxial cable.

Characteristics of Coaxial Thinnet:→

a) Cost : Less than STP
b) Installation : Inexpensive
c) Capacity : 2.5 MBPS to 10 MBPS i.e. slightly lower than thicknet
d) Range : 185 meter
e) EMI : less sensitive than UTP Cable

2) Coaxial Thicknet : It thick i.e. hard cable than thinnet coaxial. Its diameter is nearly 0.5"(inches) i.e 13mm. Since it does not bend. It has contains thick center core and it carries more signals at a larger distance. This is expensive than thinnet coaxial cable.

Characteristics of Coaxial Thicknet:→

a) Cost : Greater than STP
b) Installation : easy
c) Capacity : 10 MBPS Higher than thinnet
d) Range : 500 meter
e) EMI : less sensitive than UTP Cable

Advantages of Coaxial Cable:→

1) It is commonalty used in n/w because available in different sizes.
2) the shielding of cable provides better resistance to EMI.
3) Attenuation is less than twisted pair cable.

Disadvantages of Coaxial Cable:→

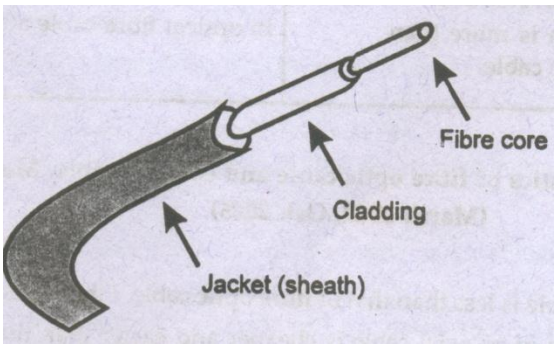
1) It is relatively expensive but less than fiber optic cable.
2) Bandwidth capacity is comparatively less than fiber optic cable.

Q) Write a short note on fiber optic cable?

a) It is a ideal cable for data transmission. The Fiber optic name suggested that center conductor of cable is fiber and term optic means the signal type in data transmission is light signal which generated by optical rays.

b) The fiber of cable is coated with cladding or gel that reflects signals back into fiber which does not effect on EMI thus this cable is free from EMI or zero sensitivity.

c) Fiber optic cable is highest speed highest bandwidth cable.



** Components of fiber optic cable:->

The fiber cable contains following types of components:

a) A center conductor:→

The center conductor of fiber optic cable is a fiber called as fiber core that consists of highly refined glass or plastic.

b) An Outer Conductor:→

It is coated with cladding or a gel that reflects signals back into fiber to reduce signal loss.

c) A plastic jacket:→

This protects cable from damage from external environment. It is called as sheath.

** Configuration of fiber optic cable:→

The are two types of fiber optic configurations such as follows:

1) Loose configuration:→

This configuration of fiber optic cable incorporates a space between the fiber sheath and the outer plastic encasement. This space is filled with a gel or other material.

2) Tight Configuration:→

This configuration contains strength wires between conductor and outer plastic encasement must supply the strength of the cable while gel or strength wires protects the delicate fiber from mechanical damage.

Characteristics of fiber optic cable:→

a) Cost : highest cost than all cable
b) Installation : difficult to install
c) Capacity : 100 MBPS
d) Range : several km of 10^S of km
e) EMI : free from EMI

Q)Comparison between Bounded or cable media or guided media:→

Properties	Twisted Pair	Coaxial Cable	Fiber Optic Cable
Cost	Inexpensive	Twice or thrice than twisted pair	Expensive
Installation	Easy	Easy	Difficult
Attenuation	More	More	Very less than all
EMI effect	Maximum	Minimum	No effect or free from EMI
Bandwidth	1 To 100 MBPS and 100 meter	500 MBPS and 100 meter	Gega BPS/Km
Signal Type Used	Electrical	Electrical	Light Signals

Q) What is protocol? Explain the concept of TCP/IP protocol?

OR what is protocol? Write a short note on Internet protocol?

**Protocol:→ A protocol is a set of rules and formats for sending and receiving data.

** Internet protocol OR TCP/IP :→

The standard protocol for the internet is called as TCP/IP i.e. transmission control protocol/Internet protocol.

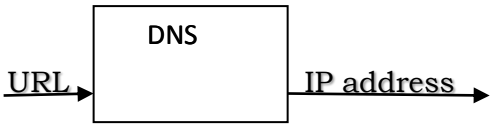
** Features of TCP/IP OR functions of TCP/IP:→

There are two functions as stated below:

1) Identify sending and receiving devices.
2) Reformatting information for transmission across internet.

1) Identification:-- Every computer on internet has a unique numeric address is called as an IP address i.e internet protocol address.

To convert text-based addresses to numeric IP address to numeric IP address TCP/IP uses DNS (Domain Name System).



In above figure URL (uniform resource locator) it is address in text based

e.g www.yahoo.com

This address of URL converted by DNS into logical address called as IP address.

2) Reformatting:→ When information sent or transmitted across internet usually travels through numerous interconnected n/w(s), before the message is sent it is reformatted or broken down into small packets or frames, this process is known as reformatting.

Each packet is then sent separately over the internet possibly travelling different routes to one common destination. At receiving end the packets are resembled into the correct order.

Q) What is topology? What are basic categories of topology?

** Topology:→ Topology is a map of n/w. It describes the arrangement of n/w. Such that how nodes, cables and connectivity devices are connected. Thus topology defines the structure of n/w.

** Basic Categories of Topology:→

There are two basic categories of topology is as defined follows:

1) Physical Topology :→ This topology describes actual layout of the n/w transmission media. It defines the way of n/w looks.

2) Logical Topology:→ This describes the logical pathway that a signal follows as it passes among the n/w modes. It defines the data passes among the nodes.

Physical and Logical topologies can takes several forms as shown below:

1) Bus Topology
2) Ring Topology
3) Star Topology
4) Mesh or Hybrid Topology

Q) What is Bus Topology?
OR Write a short note on Bus N/w?

a) Arrangement of nodes in bus topology:-

In bus topology all devices i.e. nodes (computers and peripherals) are connected to a common shared cable called as backbone cable or bus.

Some times bus topology is also known as multi-point OR multi-drop topology because in this interconnection method a common bus is used for data transmission with bidirectional communication is provided by the bus for each node.

b) Data Transmission in Bus Topology:→

In bus n/w the bus i.e. backbone cable carries transmission message. As message arrives at bus or backbone cable then it checks whether destination address matches to its own or not. If not then message goes to next workstation or node.

c) Access method used in Bus Topology:→

The contention-based access method is used for communication between two nodes. So that each node in bus n/w are struggling for accessing media.

d) Advantages of bus n/w :→

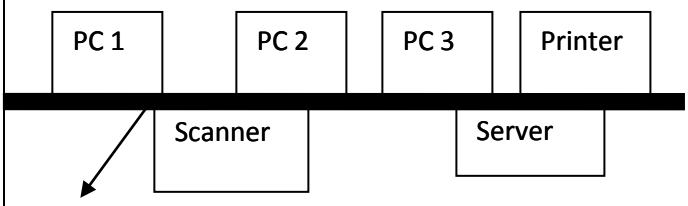
The following are the advantages of bus n/w or bus topology:

1) The bus topology is very faster than all topologies due to direct access.
2) The bus topology can be extended with sub-branches to form another topology.
3) If any node is failure then bus n/w will not disables whole system.

e) Disadvantages of bus n/w OR Bus Topology:→

The following are disadvantages provides by bus topology:

1) If bus i.e. backbone cable is failure then whole n/w is failure.
2) No controller and centrally managed.
3) Due to contention-access method each node is struggling for accessing media.



backbone cable or Bus

Q) What is Ring Topology? OR Write a short note on Ring N/w?

a) Arrangement of nodes in Ring topology:-

In ring topology all devices i.e. nodes (computers and peripherals) are connected in a ring shaped or circular manner as end to end which form a continuous loop.

b) Data Transmission in Ring Topology:→

Each node in a ring n/w sends and receive messages. The sender i.e transmitter transmits data to its nearest node i.e P.C. in that time nearest node i.e. computer is receiver it waits for data and when it receives data from sender i.e. transmitter then it then becomes transmitter if it is destination node then transmission ends if not then it sends data to

next nearest node this transmission is continues till correct destination node. Thus each node have equal access and each node circularly changes its role such as transmitter then receiver then transmitter.

c) Access method used in Ring Topology:→

The token-passing access method is used for communication between two nodes. So that each node in ring n/w utilizes a frame then sends it from transmitter to receiver until correct destination node.

d) Advantages of ring n/w :→

The following are the advantages of ring n/w or ring topology:

1) Cable failure affects limited users.
2) Each node has equal access speed to ring.
3) Cost is lowest than all topologies but caballing cost is extra.
4) The is expanded is easily anywhere.

e) Disadvantages of ring n/w OR ring Topology:→

The following are disadvantages provides by ring topology:

1) Costly wiring is required for ring topology.
2) Expensive adapter card is required.
3) Difficult connection because each node becomes one time transmitter and another time receiver then transmitter.
4) As the nodes are accessed sequentially then speed is slower.
5) If node is failure then it affects whole n/w disable.

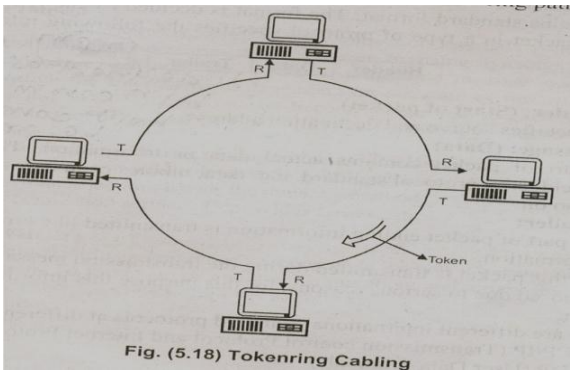


Fig. (5.18) Tokenring Cabling

Q) What is Star Topology?
OR Write a short note on Star N/w?

a) Arrangement of nodes in Star topology:-

In Star topology all devices i.e. nodes (computers and peripherals) are connected centrally to a controlling unit HUB in a star shaped manner. HUB is controller and central manager of star n/w which provides a multiport in a single line.

b) Data Transmission in Star Topology:→

When sender transmits data then central unit HUB receives this data firstly. Then HUB controls this transmission by polling i.e. Hub asks to each connecting device that whether it has message to sends or not. Each device is then in turn allowed to send its message. Then it checks destination address where data is receive then receives data to receiver and transmission ends. In this n/w only hub has highest priority.

c) Access method used in Star Topology:→

The "Polling" based access method is used for communication between two nodes. So HUB is controlling device rolled as polling device it asks each connecting device whether it sends data or not if it is then polls data from sender then matches destination node then sends data to it.

d) Advantages of star n/w :→

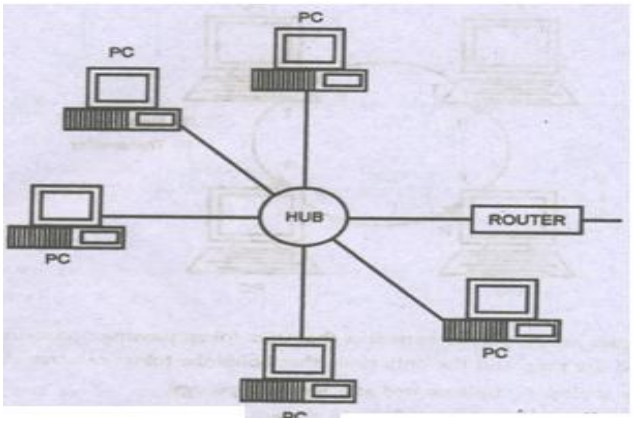
The following are the advantages of star n/w or star topology:

1) Adding a new workstation is easier than any n/w topology.
2) Control is centralized due to use of hub.
3) If one node is failure then whole system is not disables.
4) Cable failure affects limited user.

e) Disadvantages of star n/w OR star Topology:→

The following are disadvantages provides by star topology:

1) Hub fails then whole n/w fails.
2) Hub is slightly expensive.
3) Limited number of nodes are possible. Because heavy use affects speed.



Q) Which networking topology is best? Why? Explain?
OR Why star networking is best topology? Explain in detail?

The star topology is a best topology, because in star topology one computer acts as a main central computer to which all other computers are connected. That main controller or master device may be hub. It receives signals from other computers and transmits to the proper destination by checking its address. Thus actual path of travelling of signal from transmitter to receiver is decided by HUB in a star n/w.

Reconfiguration i.e. extending a new nodes is very easy, because as any computer is needed to connects directly to the server. But to make each connection long cable is needed. In star n/w any node is failure to some reason then it do not disables whole n/w.

The following are the advantages of star n/w or star topology:

1) Adding a new workstation is easier than any n/w topology.
2) Control is centralized due to use of hub.
3) If one node is failure then whole system is not disables.
4) Cable failure affects limited user.

5) Disadvantages of star n/w OR star

Q) What is a mesh topology?

a) The mesh topology is also known as hierarchical n/w or hybrid n/w. Because mesh topology incorporate all topologies.
b) In mesh topology every n/w devices has a point-to-point link to every other n/w devices.
c) A dedicated link is present in between each devices. This link carries n/w traffic only between two devices. So that it increases fault tolerance but involves extra work.
d) If media breaks then data transfer can take alternative routes. Thus caballing is complicated here.

Advantages of mesh topology:→

1) Mesh topology provides security and privacy because the message sent travels along a dedicated line.
2) It provides a point-to-point links which makes fault diagnose easily.

Disadvantages of mesh topology:-→

1)Each computer installation and reconfiguration is difficult and time consuming.
2) Requires more cost for cabling.
3) H/w is expensive because it requires to connects each link to I/O and cable.

Q) What is access method of n/w? Which are different types of access methods in networking?

" An access method is a set of rules to governing how the n/w nodes shares the transmission medium".

There are three important types of media access methods as listed below:

1) Contention Access Method.
2) Polling Access Method.
3) Token Passing Access Method

1) Contention Access Method:→

a) Contention access methods are most popular media access control method on LANs.

b) Contention access based n/w are called as probabilistic because all nodes have data surely.

c) All computers in contention based n/w are equal priority.

d) The term contention means that the computers are contending for use of the transmission medium that means in the n/w can transmits at any time i.e FIFO that means first come first serve basis.

e) Contention access method fails transmission whenever collision. The collision is occurred whenever two computers attempting to transmits at the same time. The collision is also occurred several time whenever the n/w is busy.

f) To avoid collision carrier sensing and carrier detection mechanism is used.

2) Polling Access Method:

In polling based systems there is a device is called as controller or master device to polls other devices on the n/w to see whether they are ready to transmits or receive data if it is able then routes to proper destination address.

3) Token Passing Access Method:→

In token passing access method an utilization of a frame is called as a token. A token is circulates around the n/w. A computer that needs to transmits must wait until it receives the token, when computer receives token then it is permitted to transmits. When computer completes transmitting then it passes the token frame to the next station on the token ring n/w.

Q) When token passing access method is more appropriate than contention access method?

The token passing access method is more appropriate than contention access method under the following conditions:

1) When n/w carrying time critical data then token passing access method is suitable than contention access method.

Because token passing access method results in more predictable delivery hence it is called as deterministics.

2) When n/w experience heavy utilization then token passing access method is suitable than contention access method.

Because token passing n/w(s) can not become grid locked due to excessive number of collisions.

3) When some stations should have higher priority than others then token passing access method is suitable than contention access method.

Because some token passing access method supports priority assignments.

Various Connectivity Devices in Networking of computers:-

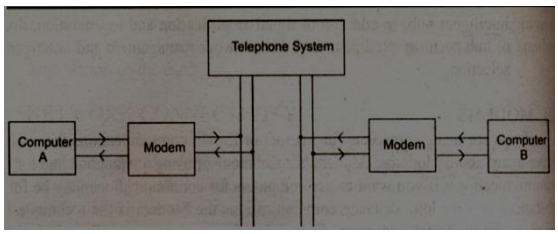
Expansion within a n/w is called as n/w connectivity. The expansion of two or more n/w(s) is called as internetwork connectivity. Thus to expand single n/w without breaking it into new parts or connecting it into other n/w(s) some standard connectivity devices are used such as :

1) Modem2) Hub 3) Repeater 4) Router

1) Modem:

Q) What is modem? Why modem is necessary in n/w? What are its advantages?

a) Modem is a internet connectivity device which interconnect computer with telephone line for digital communication as well as an internet. b) Modem is modulator and demodulator. At transmitter end is known as modulator and at receiver end it is known as demodulator. c) The modulator of modem converts computers signals or binary signals or digital signals into telephone signals or analog signals. d) The demodulator of modem converts telephone signals or analog signals into computers signals or binary signals or digital signals.



Why modem is necessary in n/w:-
OR When Modem is used:--

If computer is to connected to internet through telephone then modem as connectivity is necessary because computer transmits/receive digital signals or binary signals while telephones transmits/receive analog signals or telephone signals thus for interfacing between computer and telephone modem is necessary in n/w.

Advantages of modem:

The following are some advantages or features provided by modem:

1) Modem is used in Fax communication.
2) Modem is used in email communication in internets.
3) Modem is used in chat communication.
4) Modem is used in internet browsing.
5) Modem is high speed on analog signals so it is used in interacting between telephone and computer in n/w.
6) Modem reduces effect of noise and distortion.

Q) What are different types of modem? OR How modem is classified?

Modem is classified into two types as follows:

1) Synchronous modem.
2) Asynchronous mode

Synchronous Modem	Asynchronous Modem
1) It uses clock signals in transmission.	1) It uses bit synchronization in transmission.
2) At transmitter 'sync' and at receiver 'sync' signals are used. So it is called synchronous modem.	2) At transmitter START and at receiver STOP bit is used so it is called as asynchronous modem.
3) A wide variety of datatypes can transmitted.	3) Short messages are transmitted.
4) Transmits a long series of bits.	4) Transmits only character data.

2) Hub:

Q)What is Hub? Why Hub is necessary in n/w? What are its advantages?

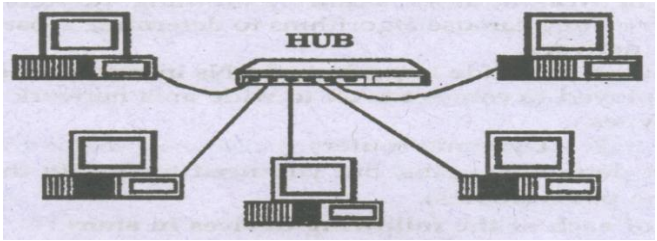
Hub is n/w connectivity device which is used in arrangement of n/w in star shaped manner.

All devices in star n/w connected to hub in centrally through a single connecting point.

Why hub is necessary in n/w OR

When Hub is used:→

The hub is necessary in arrangement of n/w in star shaped manner, that means when we wants all connection of nodes in one port and centralized management in transmission then hub is necessary so it is known as concentrator.



Functions of hub:→

Hub performs following functions:

1) Hub manages the cabling in the n/w and sends the signals to the other components of the n/w.

2) The active hub extends maximum n/w media distance. It also amplify and clean up the electronic signals.

3) The switching or intelligent hub quickly routes the signal between the ports of hub.

4) The hub accept or receives signals from transmitter then it identified receiver then after identification messages is transfer to receiver by hub.

Advantages of hub:

The hub provides following features:

1) No need of configuration of a hub.

2)Performance is fast because no processing is done at the hub.

3)Using active hub we can extends maximum n/w media distance.

4)Using switching hub or intelligent hub routing is performed i.e it determines most efficient path for sending information to receiver.

Q) What are different types of hub?

OR How hubs are classified?

There are three types of hub as listed below:

1) Passive hub

2) Active hub

3) Switching hub OR Intelligent hub

1) Passive Hub: → It is so called because it simply accepts signals and forwards them to receiver. There are no signal processing or signal regeneration.

2) Active Hub:→ It is also called as multiport repeater. An active hub so called because this hub amplify and clean up the electronic signals. The process of cleaning up is called as signal regeneration.

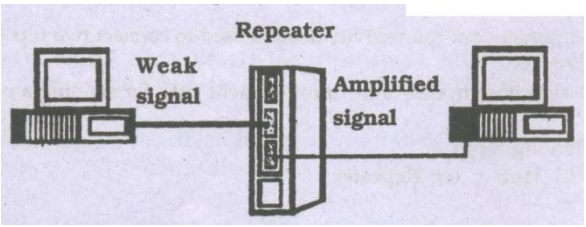
3) Switching Hub OR Intelligent Hub:→

It is also called as router hub. Because this hub accepts signal from transmitter then it performs routing i.e it determines most efficient path for sending information to receiver.

3) Repeater :-→

Q)What is Repeater? Why repeater is necessary in n/w? What are its advantages?

The repeater is a connectivity device which reshapes and amplifies the signal from transmitter to receiver.



Why repeater is necessary in n/w

OR When repeater is used:→

If the n/w is to be executed beyond predefined cable limit then repeater is used. The repeater is also used to expand or extends n/w length.

functions of repeater:

The repeater performs following type of functions:

1) Repeater extends the n/w length.

2) Repeater attaches n/w in two different floors in building.

3) Repeater reshapes the signal received from the node. The process of clean up electronic signal is called as reshape or regeneration.

4)Repeater amplifies signal from transmitter then sends to receiver.

5) If different cable medias or wireless media i.e different transmission media is used in n/w then repeater is used because repeater connects different types of transmission medias

Advantages of repeater

Repeater provides following types of features:

1) Repeater passes all traffic(multiple transmitter and receiver) in bidirections.

2) Repeater expands n/'w length.

3) Repeater handles two or more floors different networking.

Q) What are different types of repeater?
Or How repeaters are classified?

The repeater is classified into following different types:

1) Amplifiers 2) Signal Regenerating

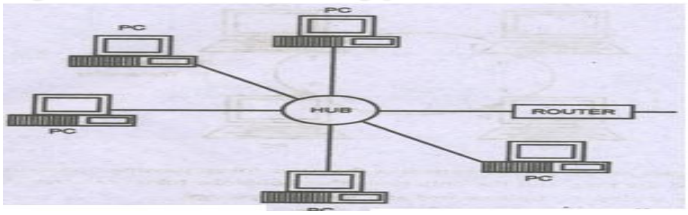
1) Amplifier: → Which is simply amplify entire incoming signals along with noise signals.

2) Signal Regenerating:→ It amplifies only data signals but it does not amplify noise signals or weak signals in n/w. It only clean up electronic signals. The process of cleaning up electronic signals is known as signal regeneration or reshape.

4) Router:→

Q)What is Router? Why router is necessary in n/w? What are its advantages?

A router is a connectivity device that examines the destination address of a message and selects themost effective route. This process is called routing. A router uses algorithm for determining path.



Why Router is necessary:-.

OR When Router is used:→

A router is used in a complex n/w i.e. similar and dissimilar topologies(arrangement of n/w) because router connects similar and dissimilar topologies. When there is WAN to LAN connection and LAN to WAN connection (in internet) then router divide large network into small n/w called subnet and it connects small n/w to large network.

Function of Routers

The router performs following type of functions:

1) Router performs routing that means it examines the destination address of a message by using algorithm and selects the most efficient or effective path for receive message to receiver. 2) Router connects two or more similar or dissimilar topologies or LANs. 3) Router divides big n/w into small n/w called as subnets and small n/w into big n/w i.e. LAN TO WAN connection.

Advantages of Router

1) Router connects LAN to WAN i.e. small n/w to large or big n/w as well as router divides large n/w into small n/w called subnet. Thus generally in internetworking router is used to connection between LAN to WAN.

2) Router provides connectivity across the WAN links.

3) Router provides multi ports for connection of nodes.

Q) What are different types of router?

OR How routers are classified?

The routers are classified into two types as follows:

1) Static Router

2) Dynamic Router

1) Static Router:→ Static router do not determines path or routes but you need to specify them manually.

2) Dynamic Router:→ Dynamic router have capacity to determine paths i.e. routes.

Q) Discuss in detail Ethernet with Ethernet terminology?

OR Write a short note on Ethernet?

a) Ethernet is also called as IEEE 802.3 (IEEE-Institute of electrical and electronics engineers) standard with CSMA/CD i.e. carrier sensing multiple access/collision detection.

b) Ethernet transmits data in small unit called as frame. Generally in this n/w contention access method is used for data transmission.

c) An Ethernet is a n/w topology is based on baseband signaling.

d) Ethernet use a passive medium like twisted pair, co-axial cable as transmission media.

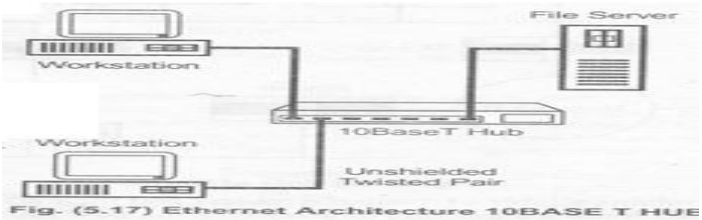


Fig. (5.17) Ethernet Architecture 10BASE T HUB

** Standard types of Ethernet OR Ethernet topologies:→

According to their data transmission speed and physical media used Ethernet classified into following standard groups :

1) 10 BASE 2 OR 10 BASE 2 Ethernet cabling

This Ethernet standard uses thinnet co-axial cable. The name of Ethernet standard begins with 10 it means that the transmission speed is 10 MBPS. The term "BASE" means that baseband signaling and 2 means two baseband signals are generated to operating.

a) Cable distance = Min 0.5 meters
= 1.5 feet.

b) The max. network segment distance
=185 meter = 607 feet.

c) The entire n/w cabling scheme cannot exceed 925 meters = 3035 feet.

2) 10 BASE 5 OR 10 BASE 5 Ethernet cabling

This Ethernet standard uses thicknet co-axial cable. The name of Ethernet standard begins with 10 it means that the transmission speed is 10 MBPS. The term "BASE" means that baseband signaling and 5 means five baseband signals are generated to operating.

a) Cable distance = Min 0.5 meters
= 1.5 feet.

b) The max. network segment distance
=500 meter = 1640 feet.

c) The entire n/w cabling scheme cannot exceed 2500 meters = 8200 feet.

3) 10 BASE T OR 10 BASE T Ethernet cabling

This Ethernet standard uses UTP cable. The name of Ethernet standard begins with 10 it means that the transmission speed is 10 MBPS. The term "BASE" means that baseband signaling and T means twisted pair wire is used.

a) Maximum number of computers on LAN is 1024.

b) The cable segment length hub to transceiver is 100 meters = 328 feet.

4) 10 BASE FL OR 10 BASE FL Ethernet cabling :→

This Ethernet standard uses Optical fiber cable. The name of Ethernet standard begins with 10 it means that the transmission speed is 10 MBPS. The term "BASE" means that baseband signaling and FL means fiber optic cable is used.

This supports the maximum cabling distance of about 2000 meters and eliminates any electrical complications.

5) 100 VG- Any LAN Ethernet cabling :→

a) Speed of transmission= 100 MBPS because cabling begins with 100.

b) In name VG suggested Voice Grade signaling is used in transmission.

c) Uses twisted pair cable.

d) Maximum length of cable attached to hub is 250 meters=820 feet.

Q) What is role of Ethernet?

OR Write a short note on role of Ethernet in n/w?

In case of Ethernet workstations sends signals in the form of packets across the n/w. When a collision takes place it stops transmissions of workstations and allows to retransmits after random internet of time. Ethernet uses CSMA/CD protocol i.e. carrier sensing multiple access/collision detection.

Q) What is multiplexing? When it is useful? What are different types of multiplexing?

Multiplexing:→ This is a technique that enables media to supports multiple data channels.

Multiplexing is useful under following circumstances:→

1) When media bandwidth is costly.

2) When band width us idle.

3) When large amount of data must be transmitted through low capacity channels.

Types of multiplexing:→

There are two types of multiplexing such as shown below:

1) Frequency Division multiplexing:→In this technique all data channels are converted to analog form. Each analog signal is modulated by a separate frequency is called as carrier frequency.

Frequency - Division Multiplexing (FDM)

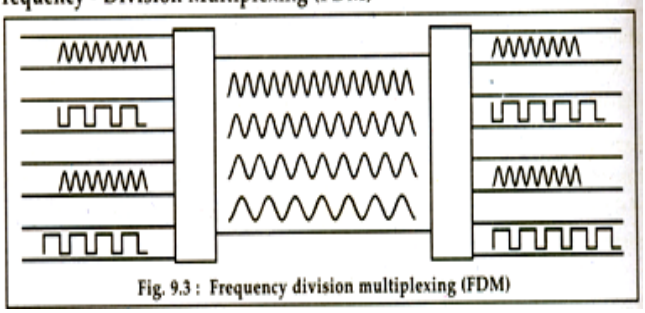


Fig. 9.3 : Frequency division multiplexing (FDM)

2) Time Division Multiplexing: TDM divides a channel into time slots that are allocated to the data streams to be transmitted. If sender and receiver agrees on time slot assignments then receiver can easily recovers and reconstructs original data streams.

Time Division Multiplexing (TDM)

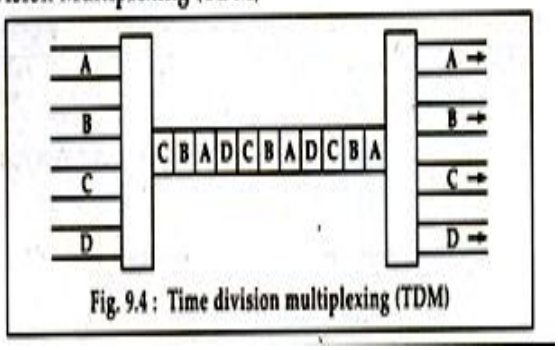


Fig. 9.4 : Time division multiplexing (TDM)

Q) What is a satellite? What are its uses?
A satellite is an artificial revolving object round the earth. It contains different communication electronic systems. It is launched for long distance as well as microwave communications. The satellite is full duplex system since it is a two-way communications. Satellite communications increases the area of coverage.

Uses of satellite:

1) Telecommunication system.

2) Meteorological information.

3) Cellular phones.

4) It is used for communication over a long distance on earth.

5) Frequencies used being very high can carry enormous data due to large bandwidth. 6) Communication in polar region is possible. 7) Surveying for mineral wealth, bio wealth, forests, water etc
8) Fire in forest, floods in rivers, storms, earthquakes and other natural disasters can be predicted much earlier.
9) Weather forecasting has become more accurate.
10) Global positioning system (G.P.S.)

Chapter : NETWORKING TECHNOLOGY

Objective Type Questions asked in Board Examination

1) If N/W is to extended beyond predefined cable limit ---------- is used
a) Modem b) Repeater c) Hub d) Router (M-2002)
Ans: b) Repeater

2) The most widely used & economical cable for N/W installation is --------
a) Fiber-Optic b) UTP c) STP d) Co-axial (M-2003)
Ans: b) UTP

3) The transmission rate of --------- is typical for fiber optic cable
a) 10 MBPS b) 25 MBPS c) 100 MBPS d) 500 MBPS (O-2003)
Ans: c) 100 MBPS

4) A device used for modulation & demodulation process in N/W is ------
a) Hub b) Router c) Modem d) Repeater (M-2004)
Ans: c) Modem

5) ---------- cable type is ideal for connection of N/W(s) which are at a 10km distance
a) UTP b) STP c) Co-axial d) Fiber Optic (O-2004)
Ans: c) Co-axial

6) The transmission rate of --------- is typical for fiber optic cable
a) 10 MBPS b) 25 MBPS c) 100 MBPS d) 500 MBPS (M-2005)
Ans: c) 100 MBPS

7) The cell phone/mobile phone uses ---------- transmission technology.
a) Radio b) Microwave c) Infrared d) satellite (O-2005)
Ans: b) Microwave

8) --------- does not regenerate the computer signal in N/W(s)
a) Passive Hub b) Active Hub c) Repeater d) All the three (M-2006)
Ans: a) Passive Hub

9) ---------- cable type supports the greatest cable length for computer networking.
a) UTP b) STP c) Thicknet Co-axial d) Thinnet Co-axial (O-2006)
Ans: c) Thicknet Co-axial

10) ---------- cable has highest bandwidth.
a) UTP b) STP c) Co-axial d) Fiber-Optic (M-2007)
Ans: d) Fiber-Optic

11) The transmission rate of --------- is typical for fiber optic cable
a) 10 MBPS b) 25 MBPS c) 100 MBPS d) 5000 MBPS (O-2007)
Ans : c) 100 MBPS

12) Most widely used & economical cable for N/W installation is ---------
a) Fiber-Optic b) UTP c) STP d) Co-axial (M-2008)
Ans: b) UTP

13) If the N/W is to be executed beyond predefined cable limit ---------- is used
a) Modem b) Repeater c) Hub d) Repeater (O-2008)
Ans: d) Repeater

14) Electromagnetic Interference is minimum in case of ---------- cable
a) UTP b) STP c) Fiber Optic d) Co-axial (M-2009)
Ans : c) Fiber Optic

15) In TCP/IP is ---------- protocol
a) connectionless b) connection oriented c) Address resolution d) Datagram (O-2009)
Ans : a) connectionless

3 Marks Questions asked in Board Examination

March -2002

1) Compare the characteristics of fiber optic cable & co axial cable. Mention atleast three points

2) Define topology. Explain STAR and RING topologies with diagram.
3) Write a short note on UTP cable with its characteristics

March-2003

1) Write a note on Ethernet.
2) What are the advantages of computer N/W(s)? Distinguish between LAN and WAN?
3) Explain the following terms:
   a) MODEM b) HUB c) REPEATER
4) What is transmission media? Explain the structure of a co-axial cable?
5) Explain in short star, ring and bus topology?

Marh-2004

1) Explain in short the six important characteristics of transmission media?
2) What do you mean by N/W topology? Explain in brief the two basic categories of topologies?
3) What is HUB? Explain the active HUB and PASSIVE HUB?

March-2005

1) Compare the co-axial cable & twisted pair cable used for networking?
2) Define topology. Explain STAR and RING topology?
3) Write a short note on Ethernet?

March-2006

1) Compare STP & Co-axial cable with reference to any three characteristics of transmission media?
2) Explain router & modem with their uses.
3) Define topology? Explain STAR topology with its advantages?

March-2007

1) Compare & list any three points for the characteristics of fiber optic cable & co-axial cable
2) Which networking topology is best? Why Explain?
3) What is mean by protocol? Explain the concept of TCP/IP protocol?

March-2008

1) Compare the characteristics of fiber-optic & co-axial cable?
2) Explain RING topology & token passing
3) What is meant by protocol? Explain the concept of TCP/IP protocol?

March-2009

1) Explain the following characteristics of transmission media:
   i) Band Usage ii) Attenuation iii) Electromagnetic Interference
2) Explain twisted pair cable with a suitable figure?
3) Compare at least three characteristics of UTP & Optical Fiber cable?

Oct-2009

1) Compare between UTP and STP cable
2) Explain function of Router in Network & list different types of routers?
3) List various access methods in N/W? Explain any one method in detail?

Oct-2008

1) Compare the characteristics of fiber optic & UTP cable. Mention atleast three points?
2) Define Bus, Ring & Star topologies. Draw suitable diagram for each?
3) Explain the following access methods in brief:
   a) contention b) token passing

Oct-2007

1) Define topology? Explain STAR & BUS topologies with diagram?

2) Explain in short the six important characteristics of transmission media?
3) Explain the RING topology & token passing

Oct-2006

1) Compare Fiber optic & UTP cables with reference to any three characteristics of transmission media?
2) Explain HUB & REPEATER with their uses?
3) What do you mean by topology? Explain the BUS topology with its advantages?

Oct-2005

1) Explain bandwidth, attenuation & electromagnetic interference?
2) Compare the characteristics of fiber optic cable & co-axial cable?
3) What do you mean by computer N/W? Give any four advantages of computer N/W?

Oct-2004

1) What is Transmission Medium? What are the advantages of wireless transmission?
2) Write a note on twisted pair cable?
3) What are the contention & polling access methods?
4) What is protocol? Explain the concept of TCP/IP protocol?
5) Write a short note on LAN?

Oct-2003

1) Compare the co-axial cable with twisted pair cable. Mention atleast three points?
2) Explain the RING topology & token passing?
3) What is meant by protocol? Explain the concept of TCP/IP protocol?

4 Marks Questions asked in Board Examination

Oct-2003

1) State four LAN wireless transmission methods? Explain any two of them?
2) Writes the functions of each of the following devices in short:
   i) Modem ii) Hub iii) Repeater iv) Router

Oct-2004

1) Explain in brief the following connectivity devices:
   i) Modem ii) Hub iii) Repeater iv) Router
2) What are Network Topologies? Explain the commonly used topologies with appropriate diagrams?

Oct-2005

1) State & explain different networking media? Explain any two wireless media?
2) What are different networking devices? Explain the function of any three networking devices?

Oct-2006

1) Explain the following characteristic of transmission media:
   a) Bandwidth ii) Band Usage iii) Attenuation iv) EMI
2) Write a short note on co-axial cable with suitable figure?

Oct-2007

1) Write the function of each of the following devices in short:
   a) Modem ii) Router iii) Hub iv) Repeater
2) Compare any four attributes of UTP and Optical Fiber cable?

Oct-2008

1) Write in short the functions of each of the following devices :
   a) Modem ii) Router iii) Hub iv) Repeater

2) Write a short note on Ethernet?

Oct-2009

1) What is Topology? Give different types of network topologies? Explain Bus topology?

March-2002

1) Explain the following characteristics of transmission media:
   i) Bandwidth ii) Band Usage iii) Attenuation
   iv) Immunity from electromagnetic interference
2) Explain Hub & Repeater in detail?

March-2003

1) Discuss any two access methods of networking?

March-2004

1) Compare any four attributes of UTP & Optical Fiber cable?
2) What do you mean by protocol? Write a short note on a TCP/IP protocol?

March-2005

1) Explain any four points to justify why wireless N/W(s) are useful?
2) What is a HUB? Explain its types?

March-2006

1) What do you mean by Networking? State any three differentiation points between LAN and WAN?
2) Explain token ring & contention access methods of networking?

March-2007

1) Explain any four points to explain why wireless networks are useful?
2) Discuss any two access methods of networking?

March-2008

1) Explain the following characteristics of transmission media:
   i) Bandwidth ii) Band Usage iii) Attenuation
   iv) Immunity for electromagnetic interference
2) Write the function of each of the following devices in short:
   i) Modem ii) Repeater iii) Hub iv) Router

March-2009

1) Explain RING topology with necessary diagram & state its important advantages?
2) Explain the following devices of computer network:
   i) Modem ii) Repeater iii) Hub iv) Router

Networking Technology

Jul-17	Compare any four attribute of UTP and Fiber Optic Cable.
Jul-16	Compare any four attributes of coaxial thicknet cable with UTP cable.
Mar-13	Compare any four attributes of UTP and optical fiber cable.
Oct-12	Compare any three characteristics of twisted pair and coaxial cable.
Mar-17	Compare any three characteristics of Twisted Pair Cable with Coaxial Cable.
Mar-12	Compare at least three characteristics of UTP and STP cables.
Oct-10	Compare atleast three characteristics of Twisted Pair cable and coaxial cable.
Mar-11	Compare between UTP and Fiber Optic Cable.
Oct-14	Compare characteristics of coaxial and fiber optic cable.

Jul-17	Compare Thicknet and Thinnet Coaxial Cable. (At least 3 points).
Mar-15	Compare twisted pair cable and coaxial cable.
Oct-13	Define access method. Explain contention access method and token passing Access Method.
Mar-13	Define Bus, Ring and Star topologies. Draw simple diagram for each.
Mar-10	Define the term topology. Explain various topologies with diagram.
Oct-14	Describe various network topology with diagram.
Aug-18	Differentiate between co-axial cable and fiber optic cable.
Mar-11	Differentiate between LAN and WAN.
Oct-13	Differentiate between UTP and STP cable.
Mar-16	Distinguish between LAN and WAN.
Oct-11	Draw the diagram of fiber optic cable and explain.
Mar-14	Explain any three characteristics of Transmission Media.
Oct-10	Explain bus topology with necessary diagram and state its advantages.
Oct-10	Explain coaxial cable with a suitable figure.
Oct-13	Explain concept of the TCP/IP protocol.
Jul-16	Explain Ethernet in short. State any four Ethernet topologies.
Mar-15	Explain Ethernet Protocol used in Network.
Mar-12	Explain fiber optic cable with a suitable figure.
Mar-18	Explain fiber-optic cable with a neat diagram.
Mar-13	Explain HUB and REPEATER in detail.
Mar-10	Explain in brief 'Token Passing' and 'Polling' access methods of n/w.
Jul-17	Explain in brief following access methods : i) Polling ii) Token Passing
Oct-14	Explain in brief following connectivity devices : i) HUB ii) Repeater iii) Modem
Mar-18	Explain in brief the following access methods: i) Contention ii) Token Passing
Oct-10	Explain in brief the following characteristics of Transmission Media : i) Bandwidth ii) Cost of Media iii) Electromagnetic Interference
Mar-18	Explain in brief the following connectivity devices : i) Repeater ii) Router
Mar-12	Explain in brief the six important characteristics of Transmission Media.
Oct-12	Explain in detail the following connectivity devices: i) MODEM ii) HUB
Mar-16	Explain in short : i) Star Topology ii) Bus Topology iii) Ring Topology
Oct-13	Explain MODEM and HUB in detail.
Mar-18	Explain Ring and Star Topologies with simple diagrams.
Mar-14	Explain Ring Topology with diagram. State its two advantages.
Oct-12	Explain ring topology. Give its one advantage and disadvantage.
Oct-11	Explain Router in detail.
Mar-15	Explain Star and Bus Network Topology.
Mar-12	Explain star topology with necessary diagram. State its advantages.
Oct-15	Explain the following attributes of a Transmission Medium :

	i) Band Width ii) EMI iii) Band Usage iv) Attenuation
Oct-11	Explain the following characteristic of Transmission Media: i) Attenuation ii) EMI iii) Bandwidth
Mar-13	Explain the following characteristics of Transmission Media: i) Band Width ii) Band Usage ii) Attenuation
Oct-15	Explain the following connectivity devices : i) Router ii) Repeater
Oct-10	Explain the following devices : i) REPEATER ii) MODEM
Mar-12	Explain the following devices used in computer networking: i) MODEM ii) REPEATER
Oct-13	Explain the following wireless media in detail : i) Microwave ii) Infrared
Oct-15	Explain the operation of token ring in networking with a suitable diagram.
Mar-16	Explain the structure of Fiber Optic Cable.
Aug-18	Explain Token Passing and Polling Access Method.
Mar-14	Explain UTP cable with its any four characteristics.
Mar-15	Give advantages of fiber optic cable over an electrical cable.
Aug-18	Give any three advantages and three disadvantages of wireless media.
Mar-14	Give atleast two advantages and one disadvantage of wireless media over cable media.
Oct-14	List the 'Access Methods' and explain any one.
Mar-14	List various network access methods and explain any one of them.
Mar-18	What do you mean by Protocol? Explain the concept of TCP/IP protocol.
Mar-17	What is Ethernet? Discuss different types of Ethernet.
Mar-15	What is HUB? Explain all the types of HUB.
Mar-10	What is HUB? Give its types and explain.
Jul-16	What is meant by a Protocol? Explain the concept of TCP/IP protocol.
Oct-11	What is meant by Access Method? Explain any two Access Methods.
Mar-13	What is meant by protocol? Explain concept of TCP/IP protocol.
Oct-15	What is meant by protocol? Explain the concept of TCP/IP protocol.

Mar-10	What is MODEM? Explain synchronous and asynchronous modem.
Mar-14	What is MODEM? Explain working of MODEM and specify types of MODEMs.
Jul-16	What is MODEM? Why it is necessary? State any one real life application of MODEM.
Aug-18	What is Network? Differentiate between LAN and WAN.
Jul-17	What is Networking? State any three differentiating points between LAN and WAN.
Mar-14	What is protocol? Explain TCP/IP protocol used in network.
Mar-11	What is protocol? Explain TCP/IP protocol.
Mar-16	What is protocol? Explain the concept of TCP/IP protocol.
Mar-11	What is topology? Explain BUS and STAR topologies.
Mar-17	What is Transmission Media? Explain in short six characteristics of Transmission Media.
Oct-12	What is transmission media? Explain the following characteristics of Transmission Media: i) Bandwidth ii) Attenuation iii) EMI

Aug-18	What is Transmission Media? Give six characteristics of transmission media.
Mar-17	What is wireless media? Write any two advantages of wireless media.
Mar-10	Why wireless networks are essential? Give its reasons.
Mar-16	Write a note on Ethernet.
Oct-12	Write a short note of fiber optic cable with neat diagram.
Mar-17	Write a short note on Modem.
Mar-16	Write a short note on MODEM.
Oct-14	Write any four reasons of wireless media why it is useful.
Mar-11	Write functions of each of the following devices in short : i) MODEM ii) HUB iii) ROUTER iv) REPEATER
Jul-16	Write in short any three reasons to explain the usefulness of wireless n/w
Jul-17	Write short note on Ethernet Protocol.
Oct-11	Write short note on following: i) Micro wave Transmission ii) Radio wave Transmission